Features

- 2-Stage LNA and High Power Switch
- Bypass Switch on Second LNA Stage
- High RF Input Power:
  160 W CW @ +105°C, 2.6 GHz
- Noise Figure:
  1.2 dB @ 2.6 GHz
  1.5 dB @ 3.5 GHz
  1.8 dB @ 4.5 GHz
- Gain, High Gain Mode:
  34 dB @ 2.6 GHz
  33 dB @ 3.5 GHz
  32 dB @ 4.5 GHz
- Output IP3: 35 dBm (High Gain Mode)
- Lead-Free 5 mm 32-lead HQFN
- Integrated ESD Protection
- RoHS* Compliant

Applications

- High Power TDD 4G & 5G Basestation
- Wireless Infrastructure
- TDD-based Communication System

Description

The MAMF-011139 is a compact surface mount module containing a PIN diode switch and two low noise amplifiers assembled in a 5 mm 32-lead HQFN plastic package.

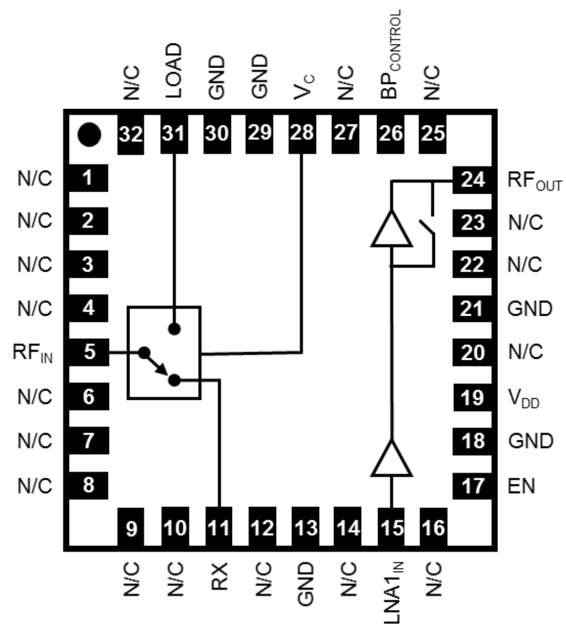
Some DC bias and matching SMT components are required for PIN switch operation and optimized noise figure. The second LNA, LNA2, may be bypassed through an integrated switch. LNA2 is powered down when bypassed.

Ordering Information[1,2]

Part Number	Package
MAMF-011139-TR1000	1K Reel
MAMF-011139-001SMB	Sample Board

1. Reference Application Note M513 for reel size information.
2. All sample boards include 3 loose parts.

Functional Schematic



Pin Configuration[3,4]

Pin #	Pin Name	Description
1-4,6-10,12,14, 16,20,22,23,25, 27,32	N/C[3]	No Connection
5	RF_{IN}	Common RF Input / Bias
11	RX	RX Switch Output
13,18,21,29,30	GND	RF Ground
15	$LNA1_{IN}$	LNA1 Input
17	EN	LNA1/2 Enable
19	V_{DD}	Drain Supply
24	RF_{OUT}	LNA2 Output
26	$BP_{CONTROL}$	Bypass Switch Control
28	V_C	RX/TX Switch Control
31	LOAD	TX Switch Output

3. MACOM recommends connecting unused package pins to ground.
4. The exposed pad centered on the package bottom must be connected to RF, DC and thermal ground.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Electrical Specifications: T_A= +25°C, V_{DD} = 5 V, $BP_{CONTROL}$ = 3.3 V, EN = 0 V
See RX/TX Switch Bias Table

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Input RF Power @ +105°C RF_{IN} - LOAD 200 mA Bias Current	2.6 GHz 3.5 GHz 4.5 GHz	W	—	160 140 125	—
Input RF Power @ +105°C RF_{IN} - LOAD 100 mA Bias Current	2.6 GHz 3.5 GHz 4.5 GHz	W	—	120 105 95	—
Switch Insertion Loss RF_{IN} - LOAD	2.6 GHz 3.5 GHz 4.5 GHz	dB	—	0.3 0.4 0.6	— 0.7 —
Noise Figure in Both Modes RF_{IN} - RF_{OUT}	2.6 GHz 3.5 GHz 4.5 GHz	dB	—	1.2 1.5 1.8	— 1.9 —
Input Return Loss in Both Modes RF_{IN} - RF_{OUT}	2.6 GHz 3.5 GHz 4.5 GHz	dB	—	12 22 12	—
Output Return Loss in Both Modes RF_{IN} - RF_{OUT}	2.6 GHz HG / LG 3.5 GHz HG / LG 4.5 GHz HG / LG	dB	—	10/17 15/13 15/17	—
Gain in High Gain Mode RF_{IN} - RF_{OUT}	2.6 GHz 3.5 GHz 4.5 GHz	dB	— 29.5 —	34.1 32.5 32.0	—
Gain in Low Gain Mode RF_{IN} - RF_{OUT}	2.6 GHz 3.5 GHz 4.5 GHz	dB	— 17 —	20.1 19.3 18.0	—
Isolation RF_{IN} - $LNA1_{IN}$	Switch State = RF_{IN} - LOAD 2.6 GHz 3.5 GHz 4.5 GHz	dB	—	46 47 45	—
Output IP3 in High Gain Mode RF_{IN} - RF_{OUT}	P_{OUT} = +10 dBm per tone, 11 MHz spacing	dBm	—	35	—
Output IP3 in Low Gain Mode RF_{IN} - RF_{OUT}	P_{OUT} = +3 dBm per tone, 11 MHz spacing	dBm	—	29.5	—
Output P1dB in High Gain Mode	RF_{IN} - RF_{OUT}	dBm	—	19	—
Output P1dB in Low Gain Mode	RF_{IN} - RF_{OUT}	dBm	—	15.3	—
V_{DD} Bias Current	High Gain Mode Low Gain Mode	mA	—	108 44	—
Control Voltage	Logic High Logic Low	V	1.2 0	—	3.45 0.6
Logic Input Current	Logic High Logic Low	µA	—	60 0.01	—

RX/TX Switch Bias Table

RF_{IN} – LOAD	RF_{IN} – RF_{OUT}	LOAD	RX	Vc	RF_{IN}
ON	OFF	0 V (-100 mA)	+48 V (10 mA)	0 V (-10 mA)	5 V (100 mA)
OFF	ON	+48 V (0 mA)	0 V (-100 mA)	+48 V (0 mA)	5 V (100 mA)

LNA Logic Truth Table[5]

Mode	EN	$BP_{CONTROL}$	Note
High Gain mode	Low	Low	LNA1 and LNA2 ON, Bypass Switch OFF
Low Gain mode	Low	High	LNA1 ON, LNA2 OFF, Bypass Switch ON
High Isolation mode	High	Low	LNA1 and LNA2 OFF, Bypass Switch OFF
Low Isolation mode	High	High	LNA1 and LNA2 OFF, Bypass Switch ON

5. If V_{DD} pin is used to turn the LNAs ON and OFF, the logic pins need to stay at Logic Low during V_{DD} ramp up and ramp down.

Absolute Maximum Ratings[6,7,8]

Parameter	Absolute Maximum
RF Input Power RF_{IN} - RX $LNA1_{IN}$ - RF_{OUT} RF_{IN} - LOAD	49 dBm @ 85°C 19 dBm See Power Derating Curves
Switch Reverse Voltage (RF & DC)	160 V
Control Voltage	Lower of 3.6 V and V_{DD}+0.5 V
V_{DD}	5.5 V
Junction Temperature Switch LNA[9]	+175°C +150°C
Case (Paddle) Temperature	-40°C to +120°C
Storage Temperature	-55°C to +150°C

6. Exceeding any one or combination of these limits may cause permanent damage to this device.
7. MACOM does not recommend sustained operation near these survivability limits.
8. Operating at nominal conditions with $T_J \le +150°C$ (LNA) and $T_J \le +175°C$ (Switch) will ensure MTTF >> 1 x 10^6 hours.
9. LNA Junction Temperature (T_J) = $T_C + \Theta_{JC} * (P_{DISS})$ where P_{DISS} is the total DC & RF dissipated power.
   - LNA: Typical thermal resistance (Θ_{JC}) = 33.4 ºC/W.

Handling Procedures

Please observe the following precautions to avoid damage:

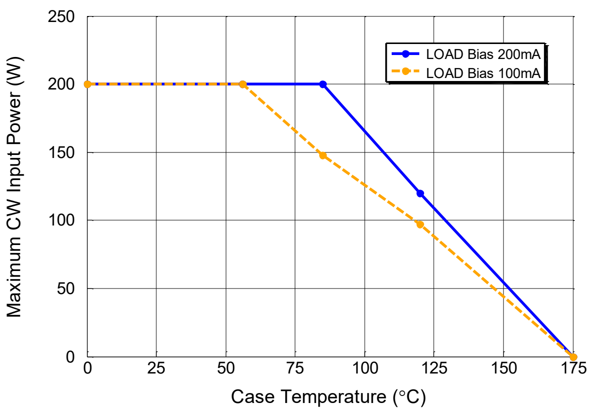
Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity.

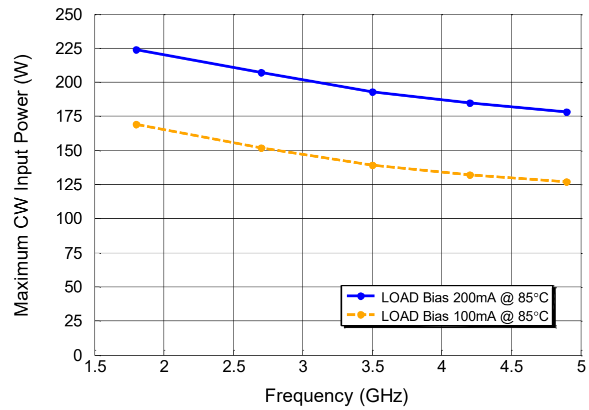
Parameter	Rating	Standard
Human Body Model (HBM)	Class 1B	ESDA/JEDEC JS-001
Charged Device Model (CDM)	Class C3	ESDA/JEDEC JS-002

Typical Performance Curves
V_{DD} = 5 V, T_C = +25°C, Z_0 = 50 Ω (unless otherwise indicated)

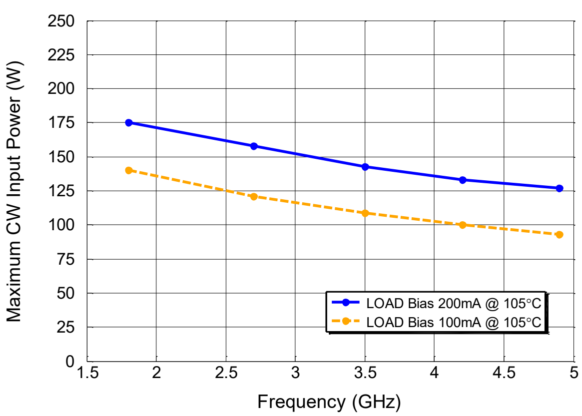
ANT to LOAD Input Power Derating Curve @ 2.7GHz



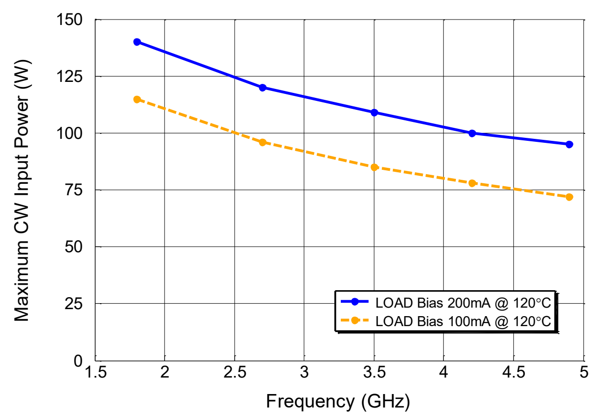
ANT to LOAD Input Power Derating Curve over Frequency @ 85°C Case Temp



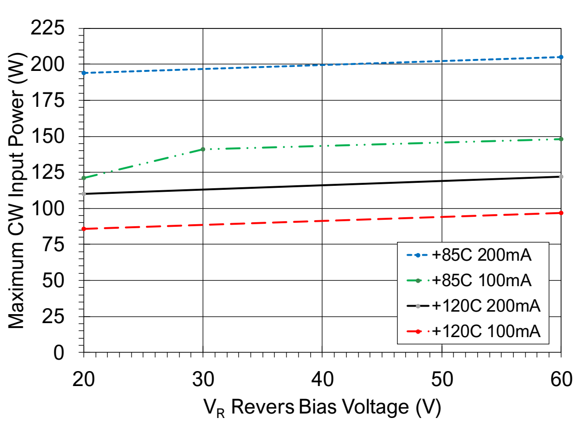
ANT to LOAD Input Power Derating Curve over Frequency @ 105°C Case Temp



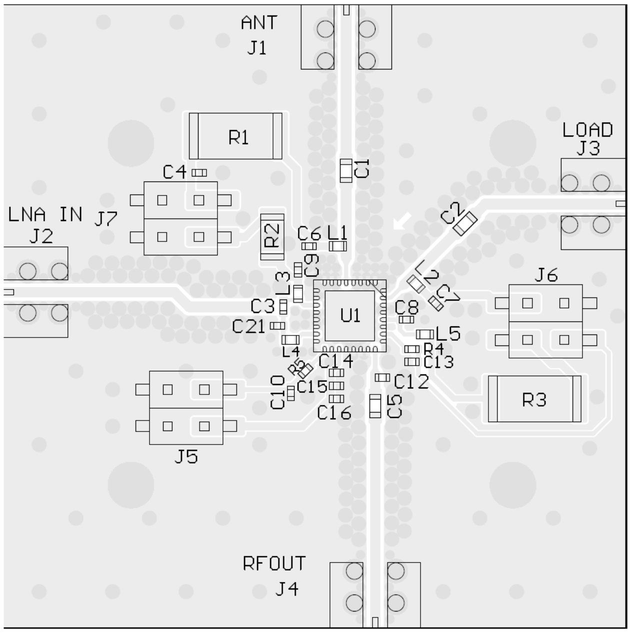
ANT to LOAD Input Power Derating Curve over Frequency @ 120°C Case Temp



ANT to LOAD Input Power Derating Curve over Reverse Bias Voltage @ 2.7GHz



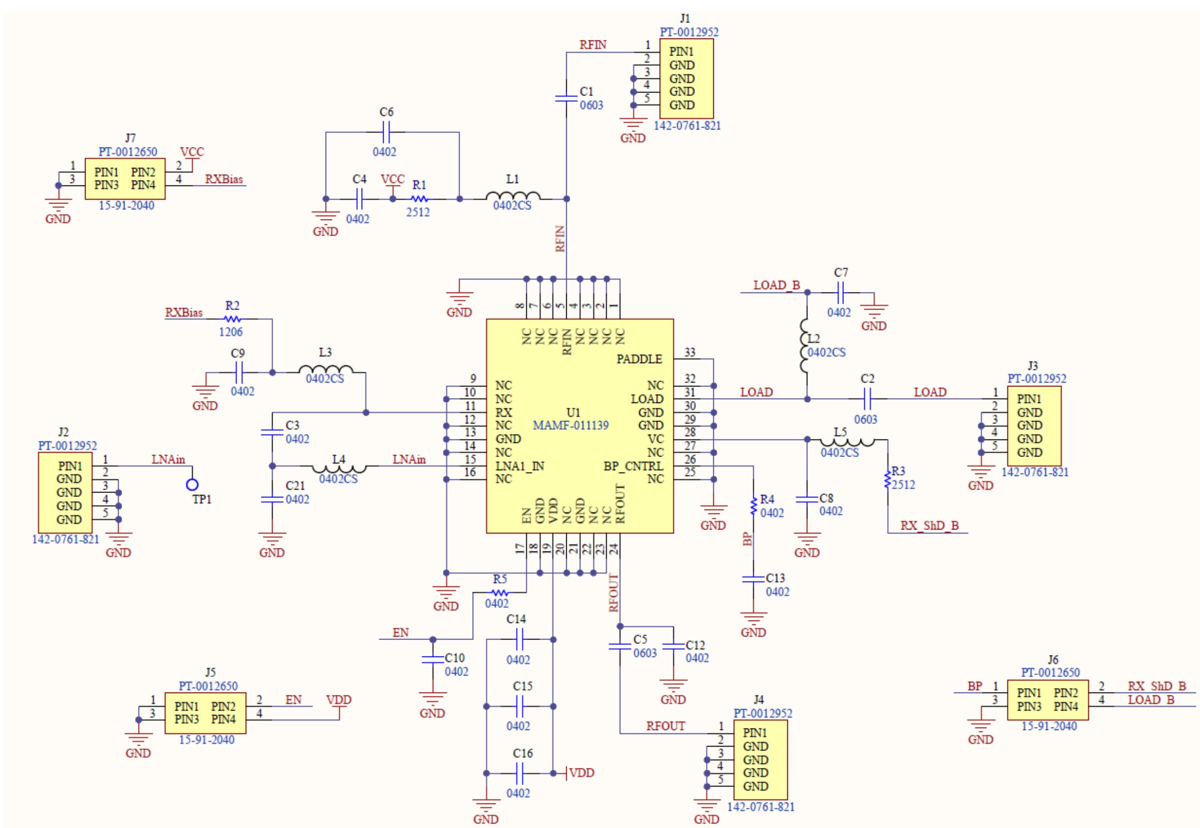
PCB Layout



Parts List

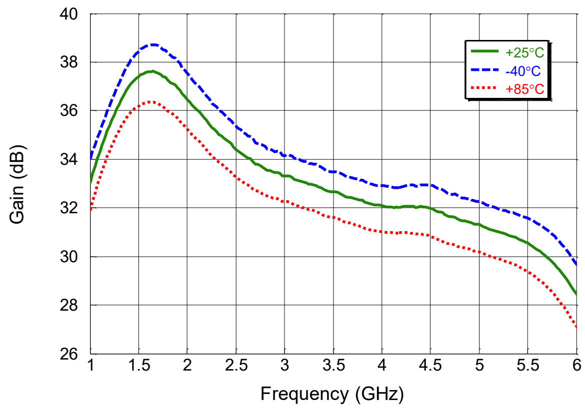
Part	Value	Case Style (Min Rating)
C1,C2	6.8 pF	0603 (≥250V)
C3	10 pF	0402 (≥100V)
C5	15 pF	0603
C4,C14	0.1 µF	0402
C6,C7,C8,C9	15 pF	0402 (≥100V)
C10	4.7 pF	0402
C12,C13,C15,C16	DNP	0402
C21	0.4 pF	0402
L1,L2,L3,L5	33 nH	0402
L4	Jumper	0402
R1	40.2 Ω	2512 (≥1W)
R2	0 Ω	1206
R3	4.7 kΩ	2512 (≥1W)
R4	0 Ω	0402
R5	100 Ω	0402

Application Schematic

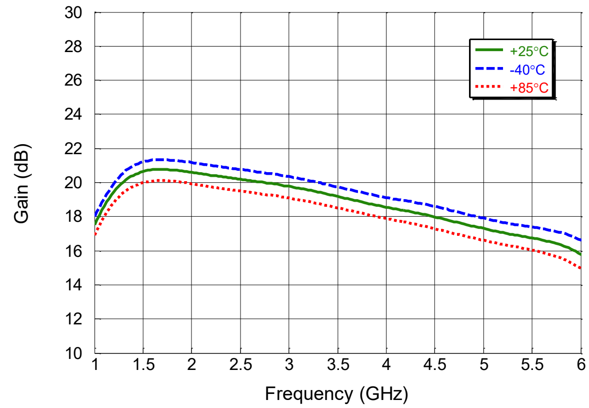


Typical Performance Curves
P_{IN} = -35 dBm, V_{DD} = 5 V, T_C = +25°C, Z_0 = 50 Ω (unless otherwise indicated)

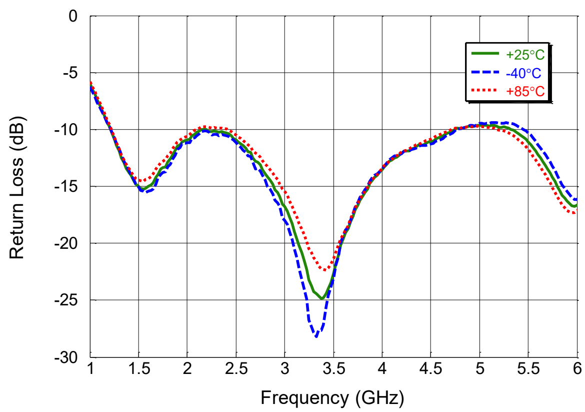
LNA Gain over swept Frequency (& Temp.) in High Gain Mode



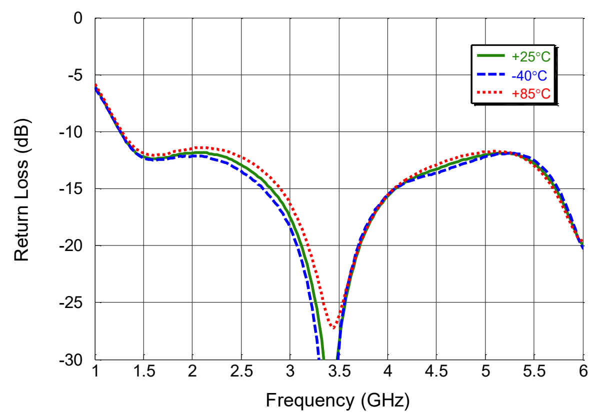
LNA Gain over swept Frequency (& Temp.) in Low Gain Mode



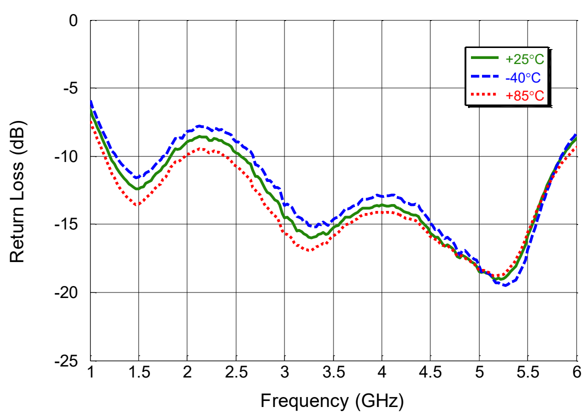
RF_{IN} Port Return Loss over swept Frequency (& Temp.) in High Gain Mode



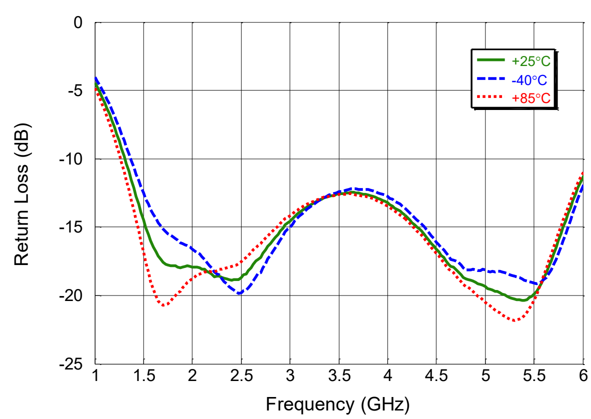
RF_{IN} Port Return Loss over swept Frequency (& Temp.) in Low Gain Mode



RF_{OUT} Port Return Loss over swept Frequency (& Temp.) in High Gain Mode



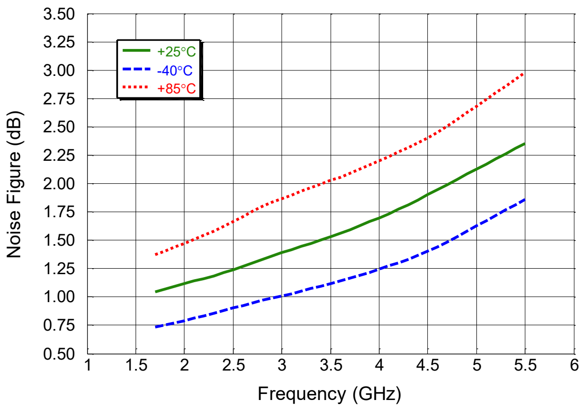
RF_{OUT} Port Return Loss over swept Frequency (& Temp.) in Low Gain Mode



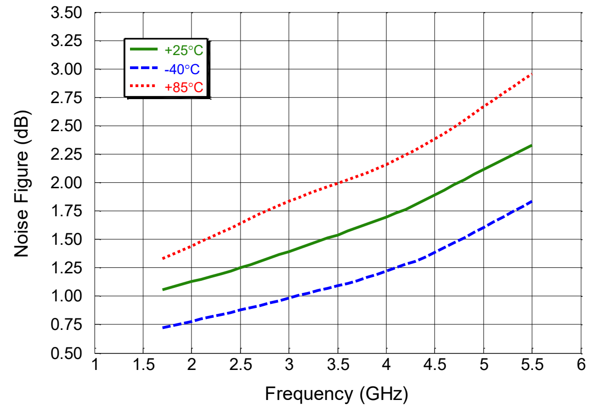
Typical Performance Curves

P_{IN} = -35 dBm, V_{DD} = 5 V, T_C = +25°C, Z_0 = 50 Ω (unless otherwise indicated)

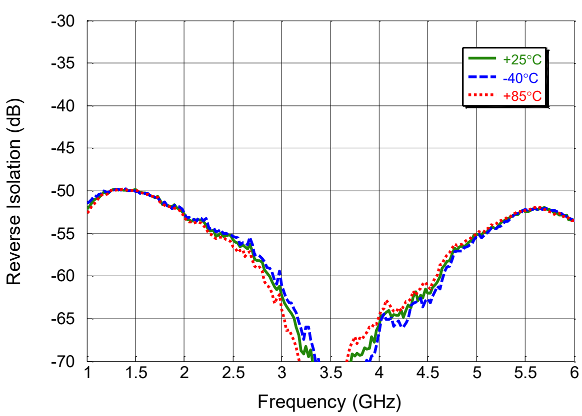
LNA Noise Figure over swept Frequency (& Temp.) in High Gain Mode



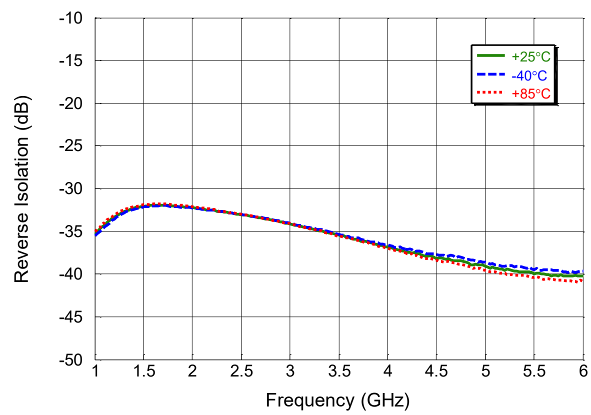
LNA Noise Figure over swept Frequency (& Temp.) in Low Gain Mode



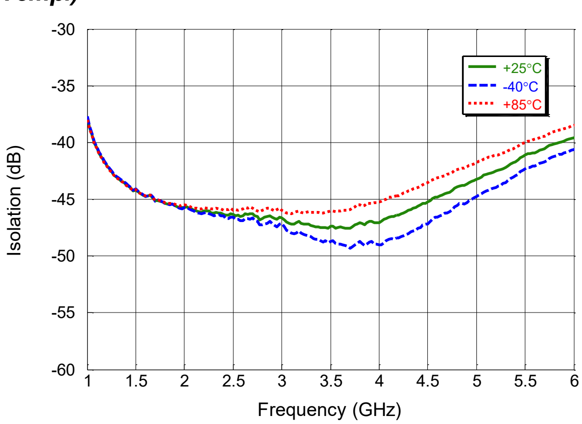
LNA1$_{IN}$ to RF$_{OUT}$ Isolation over swept Frequency (& Temp.) in High Gain Mode



LNA1$_{IN}$ to RF$_{OUT}$ Isolation over swept Frequency (& Temp.) in Low Gain Mode

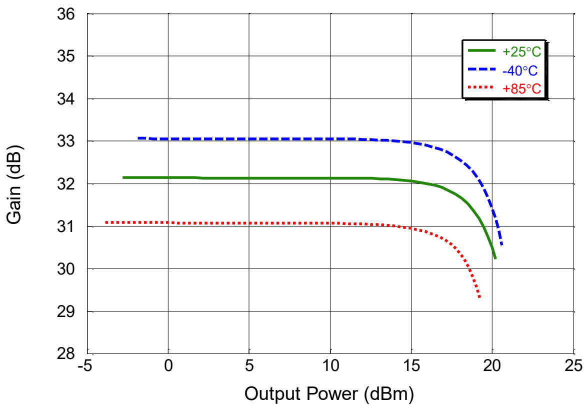


RF$_{IN}$ to LNA1$_{IN}$ Isolation over swept Frequency (& Temp.)

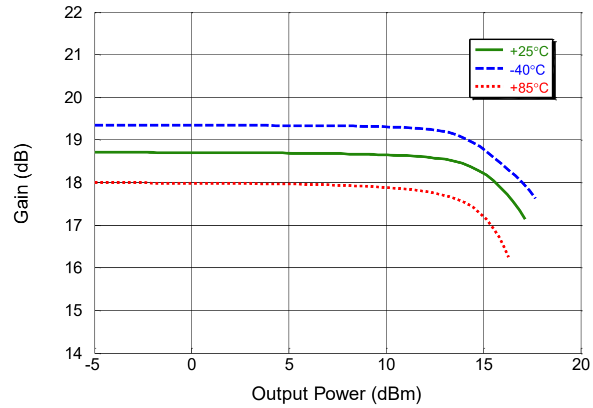


Typical Performance Curves
P_{IN} = -35 dBm, V_{DD} = 5 V, T_C = +25°C, Z_0 = 50 Ω (unless otherwise indicated)

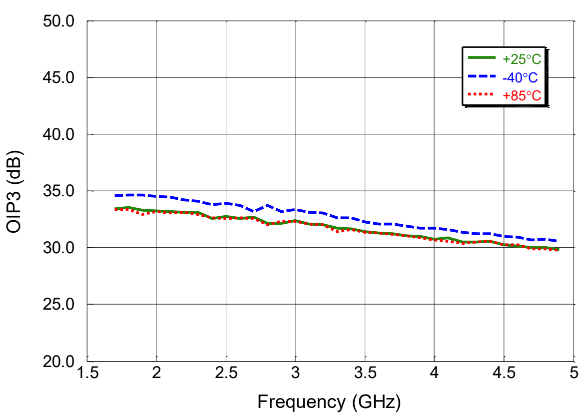
LNA Gain over swept Output Power (& Temp.) at 3.5 GHz in High Gain Mode



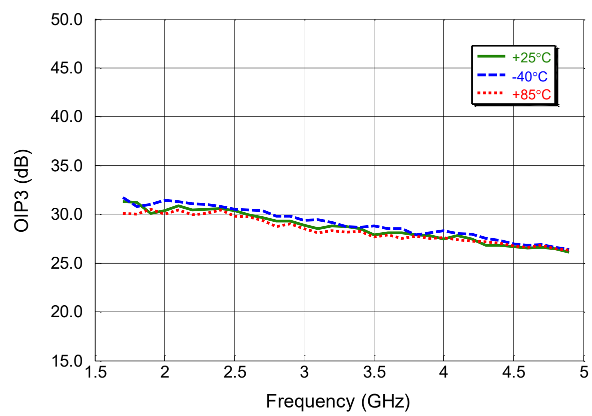
LNA Gain over swept Output Power (& Temp.) at 3.5 GHz in Low Gain Mode



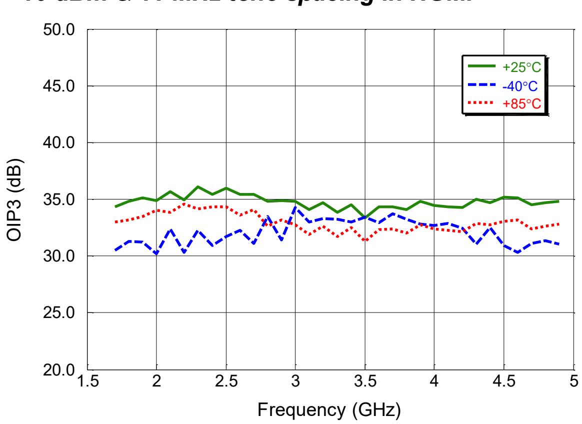
OIP3 over swept Frequency (& Temp.) with P_{IN}/Tone = -35 dBm & 10 MHz tone spacing in HGM.



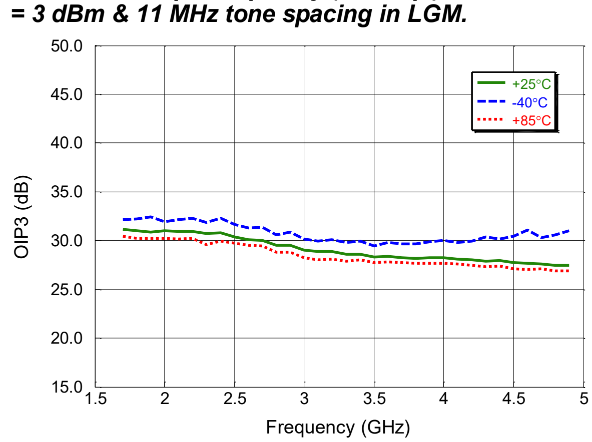
OIP3 over swept Frequency (& Temp.) with P_{IN}/Tone = -25 dBm & 10 MHz tone spacing in LGM.



OIP3 over swept Frequency (& Temp.) with P_{OUT}/Tone = 10 dBm & 11 MHz tone spacing in HGM.

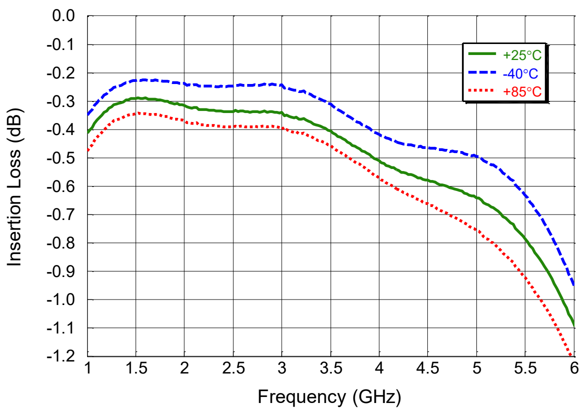


OIP3 over swept Frequency (& Temp.) with P_{OUT}/Tone = 3 dBm & 11 MHz tone spacing in LGM.

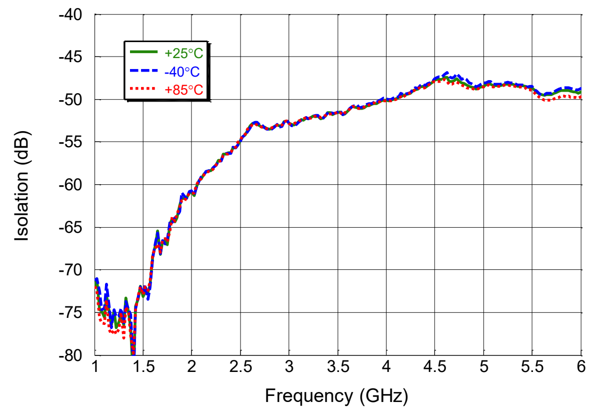


Typical Performance Curves
P_{IN} = -10 dBm, V_{DD} = 5 V, T_C = +25°C, Z_0 = 50 Ω (unless otherwise indicated)

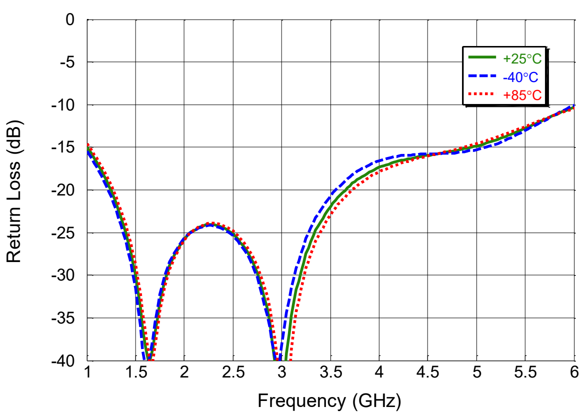
Switch Insertion Loss over swept Frequency (& Temp.)



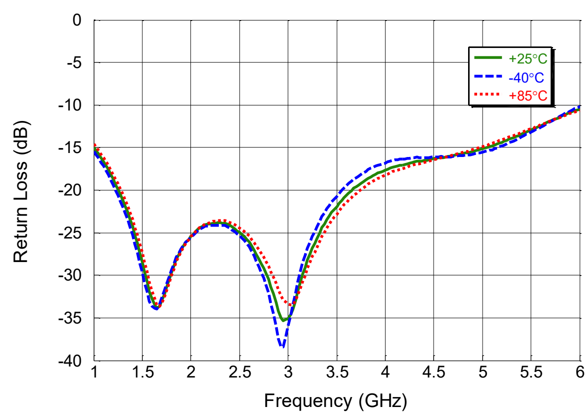
RF_{IN} to RF_{OUT} Isolation over swept Frequency (& Temp.)



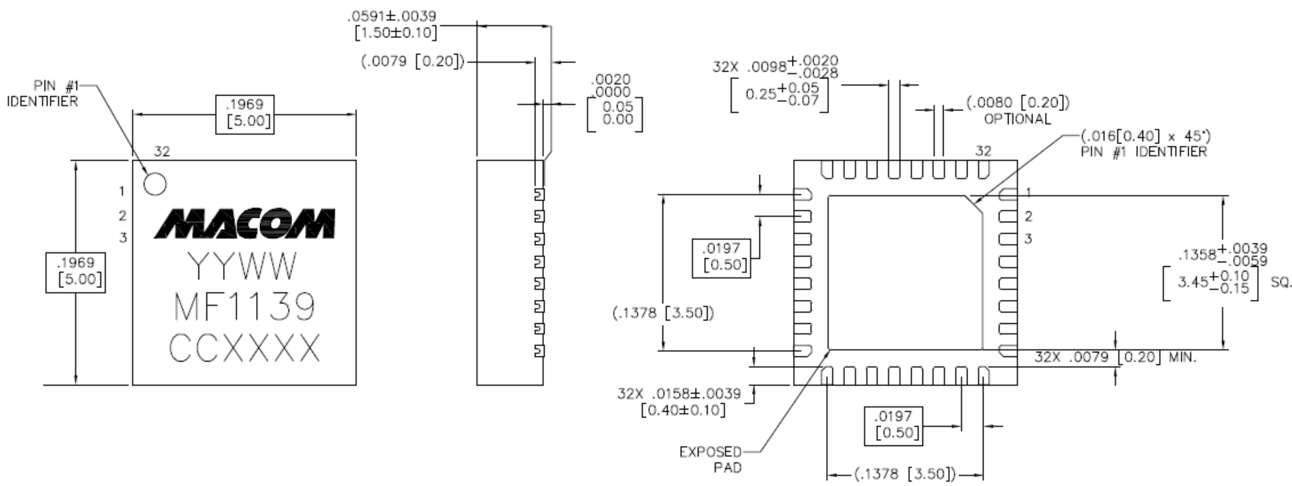
RF_{IN} Port Return Loss over swept Frequency (& Temp.)



LOAD Port Return Loss over swept Frequency (& Temp.)



Lead-Free 5 mm 32-Lead HQFN†



ALL DIMENSIONS SHOWN AS in[mm]

† Reference Application Note M538 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level 1 requirements.
Plating is NiPdAuAg.