Designing with UnitedSiC FETs

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Manager Device Technology Development

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UnitedSiC
Simply More Efficient

Contents

- Introduction to the UnitedSiC FET portfolio
- General Gate Drive Guidelines
- Using snubbers to manage switching waveforms
- Benefits of packages with Kelvin connections
- UnitedSiC FET User Guide
- Tips for paralleling TO packages

SiC Application Growth

Server & Datacenter

Lighting & Electronic Ballast

Electric Vehicles

Lab & Din Rail PSU

Battery Charging

Renewable Energy & Storage

UnitedSiC

Key Features

UnitedSiC

UJ3C & UF3C Series, 650/1200V SiC FETs

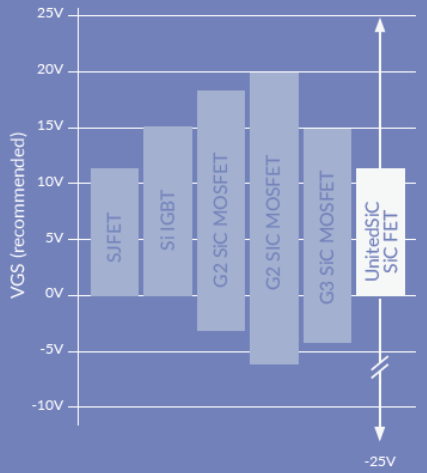
Key Features

- Excellent body diode performance (Vf < 2V)
- Drive with any Si and/or SiC gate drive voltage
- High performance cascode configuration
- Superior thermal performance
- Integrated ESD and gate protection
- Kelvin package (UF3C Fast series)

Drop-in Functionality Without Changing Gate Drive Voltage

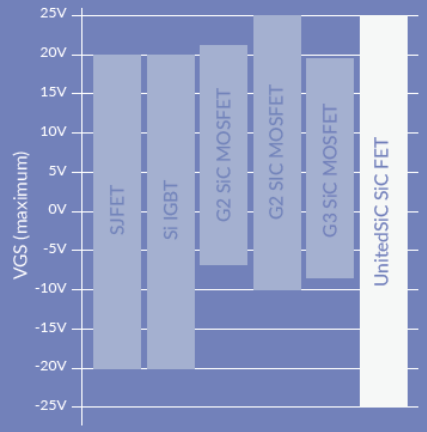
(Replaces Si IGBTs, Si FETs, SiC MOSFETs or Si Superjunction Devices)

12V/0V Operation Simplifies Upgrading



Innovative cascode configuration enables Si and SiC gate voltage compatibility

Superior Gate and ESD Protection



Integrated clamping diode protects gates from |25V| and adds ESD protection

UnitedSiC

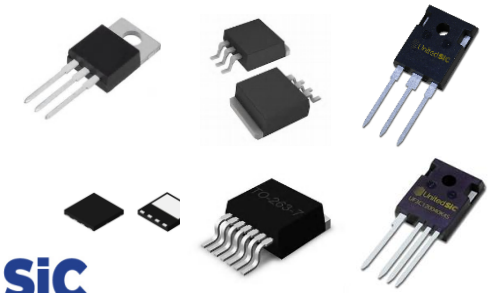
UnitedSiC Product Portfolio

UnitedSiC

- Schottky Diodes
- JFETs
- FETs
  - UJ3C — Soft Switched
  - UF3C — Hard Switched
    - 3-Leaded packages
    - Source Kelvin Packages

- Co-packaged high-performance Gen3 SiC JFETs with cascode-optimized MOSFET
- Only standard gate drive SiC device in the market today

- 650V and 1200V
- Low on-resistance RDS(on)
- Excellent reverse recovery
- Low gate charge
- Enhanced Thermal Performance
- ESD protected, HBM class 2
- T (max op) = 175°C



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UF3C performance benefits

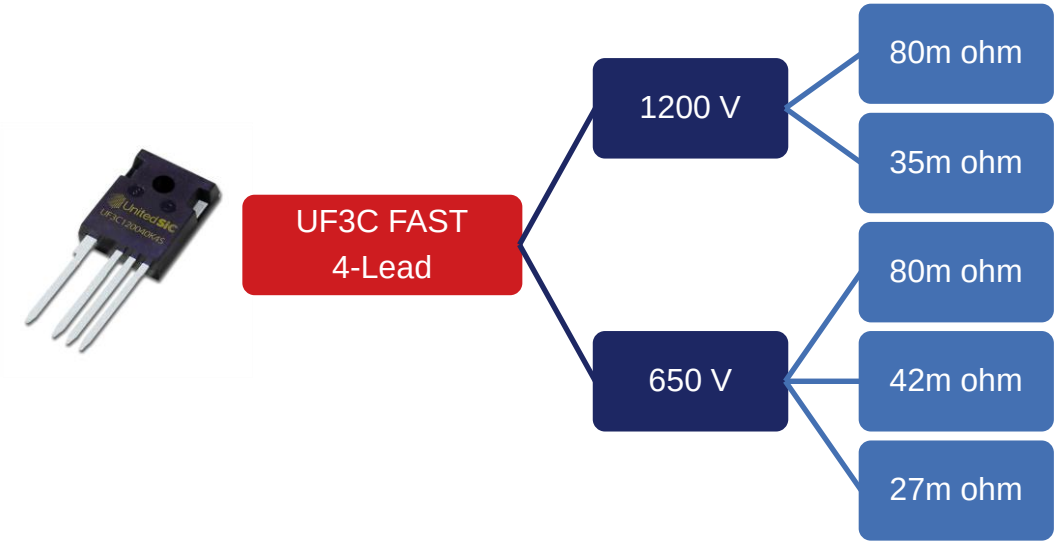
1200V Devices	UJ3C120040K3S	UF3C120040K3S
Qrr (150°C)	482nC	289nC
Rds(on)	35mohm	35mohm
VF(20A)	1.5V	1.5V

650V Devices	UJ3C065030K3S	UF3C065030K3S
Qrr (150°C)	400nC	188nC
Rds(on)	27mohm	27mohm
VF(20A)	1.3V	1.3V

- Lower losses for higher frequency switching circuits, especially where hard switching at turn-on is needed
- No changes to thermal resistance or current ratings

UnitedSiC

UF3C FAST SiC FETs in 4-lead kelvin connected package



All the benefits of UnitedSiC SiC FETs

PLUS

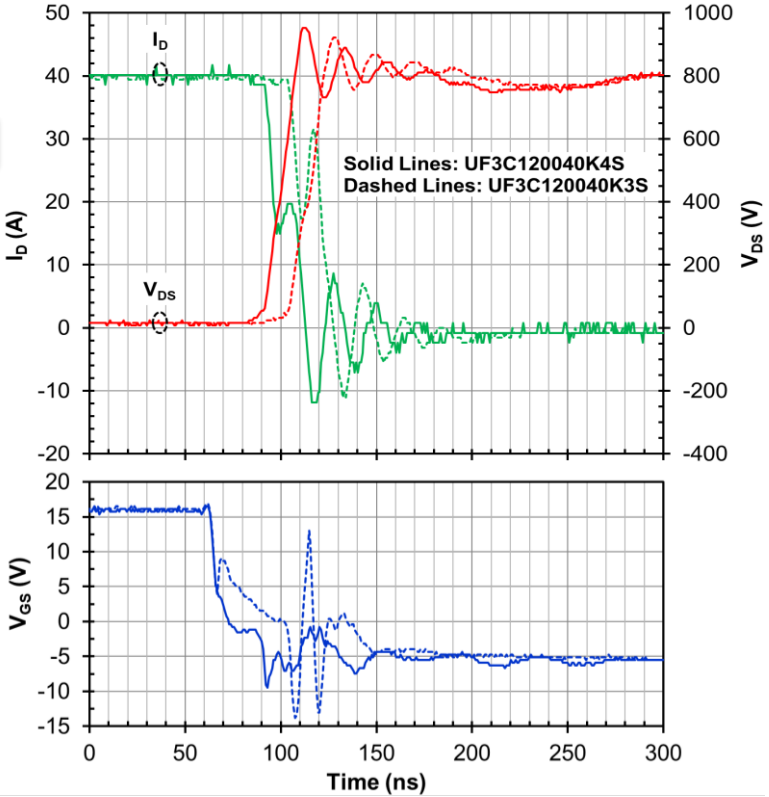
- *Extremely fast switching*
- *Lowest switching losses*
- *Clean gate waveforms*
- *No false triggering*

UnitedSiC

Turn-off Waveforms

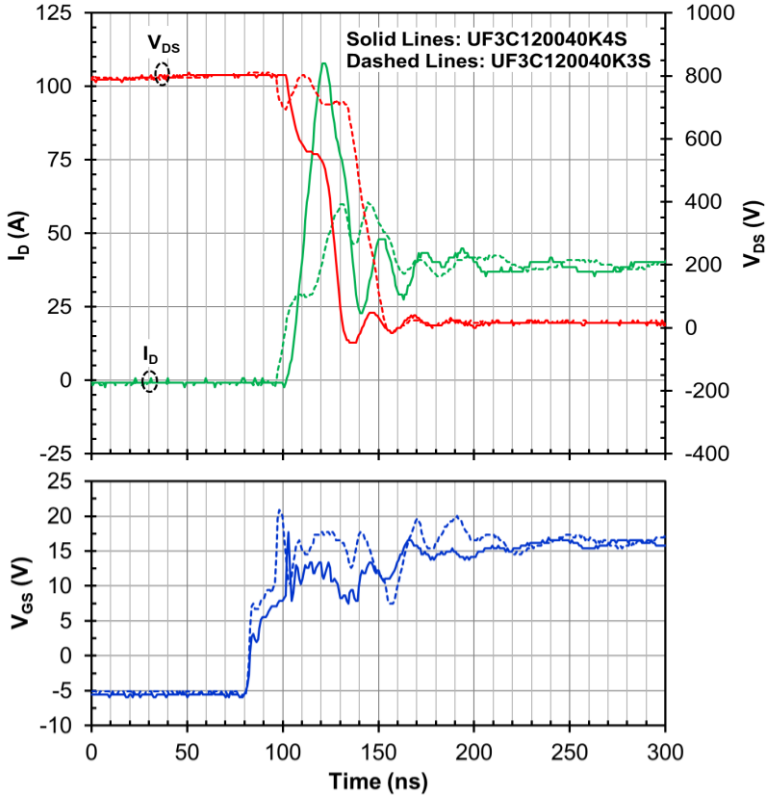
UF3C120040K3S

UF3C120040K4S



- UF3C120040K3S: E_{off} = 208µJ
- UF3C120040K4S: E_{off} = 170µJ

Turn-on Waveforms



- UF3C120040K3S: E_{on} = 1300µJ, di/dt = 3800A/µs
- UF3C120040K4S: E_{on} = 845µJ, di/dt = 7100A/µs

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800V, 40A, Half-bridge, RT, Rgon = 3Ω, Rgoff= 10Ω, FWD: Vgs = -5V, Rg = 10Ω; R_{SNUB}=10Ω, C_{SNUB}=220pF

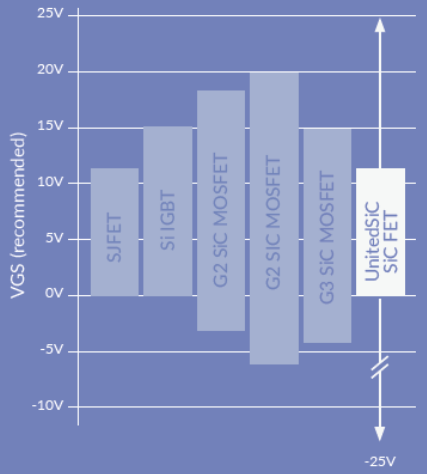
General Gate Drive Guidelines

- UnitedSiC cascode FET Vth=5V
- Vgsmax = +/-25V
- Gate drive 0 to 12V is best, especially in ZVS applications
- No issues with negative gate drive. Any voltages +/-20V may be used with the right Rg changes
- Devices are compatible with a wide range of gate drives and gate drive ICs – both Si MOS/IGBT drivers as well as newer SiC MOSFET drivers
- Also compatible with simple gate drive transformers

Drop-in Functionality Without Changing Gate Drive Voltage

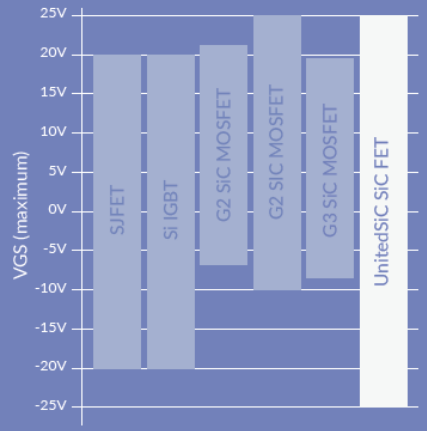
(Replaces Si IGBTs, Si FETs, SiC MOSFETs or Si Superjunction Devices)

12V/0V Operation Simplifies Upgrading



Innovative cascode configuration enables Si and SiC gate voltage compatibility

Superior Gate and ESD Protection



Integrated clamping diode protects gates from |25V| and adds ESD protection

Cascode switching and gate charge

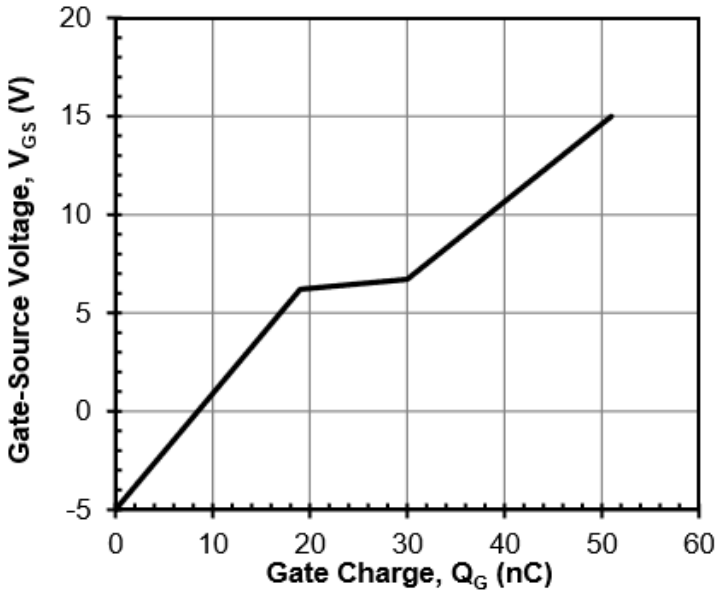
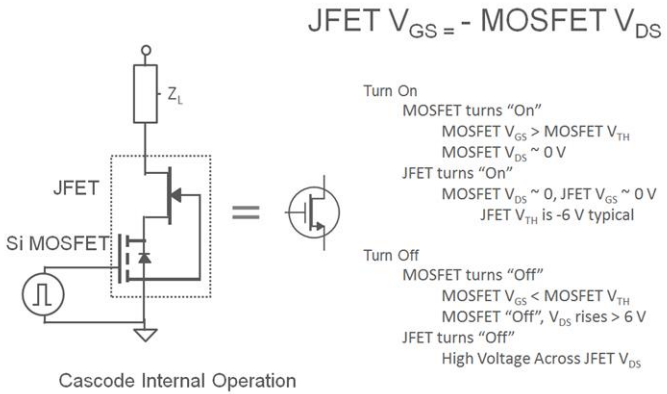
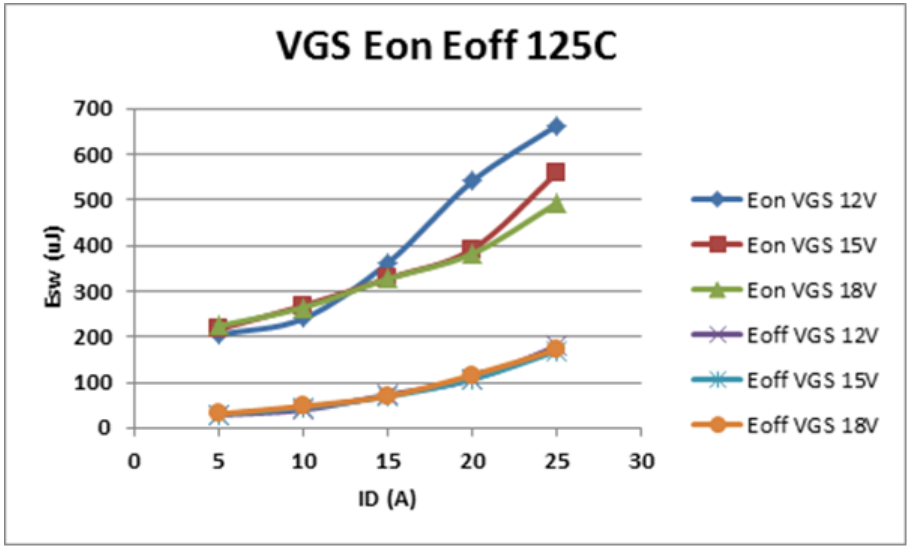


Figure 8 Typical gate charge at V_{DS} = 800V and I_D = 40A



- Gate charge comes from the LVMOS
- Same LVMOS used across many products leads to same Qg across many products
- Cascode dV/dt is controlled primarily by JFET built-in Rg (fixed) and secondarily by external MOSFET Rg (user controlled)
- Generally, turn-off is much faster than turn-on in cascodes, so it needs a higher Rgoff

V_{GS} Effect on E_{SW} for TO247-3L



HALF BRIDGE
UJ3C120080KS
HS+LS

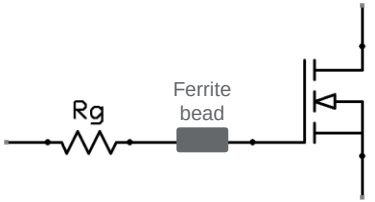
Rgon=1ohm
Rgoff=20ohm
Both HS and LS

Tj=125C

At higher currents, a Vgs>12V allows faster turn-on for lower Eon.

Not much difference below 15A

Comparison of Switching Losses with and without using Ferrite Bead



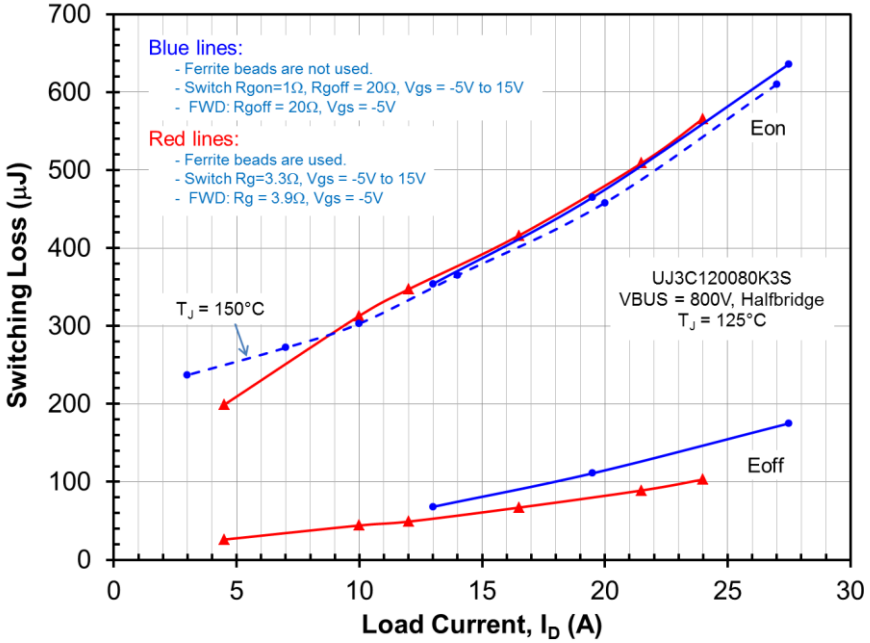
Part #: BLM41PG600SN1L
Description: FERRITE BEAD 60 OHM 1806 1LN

Looks like 100nH at 100MHz

3. Rating

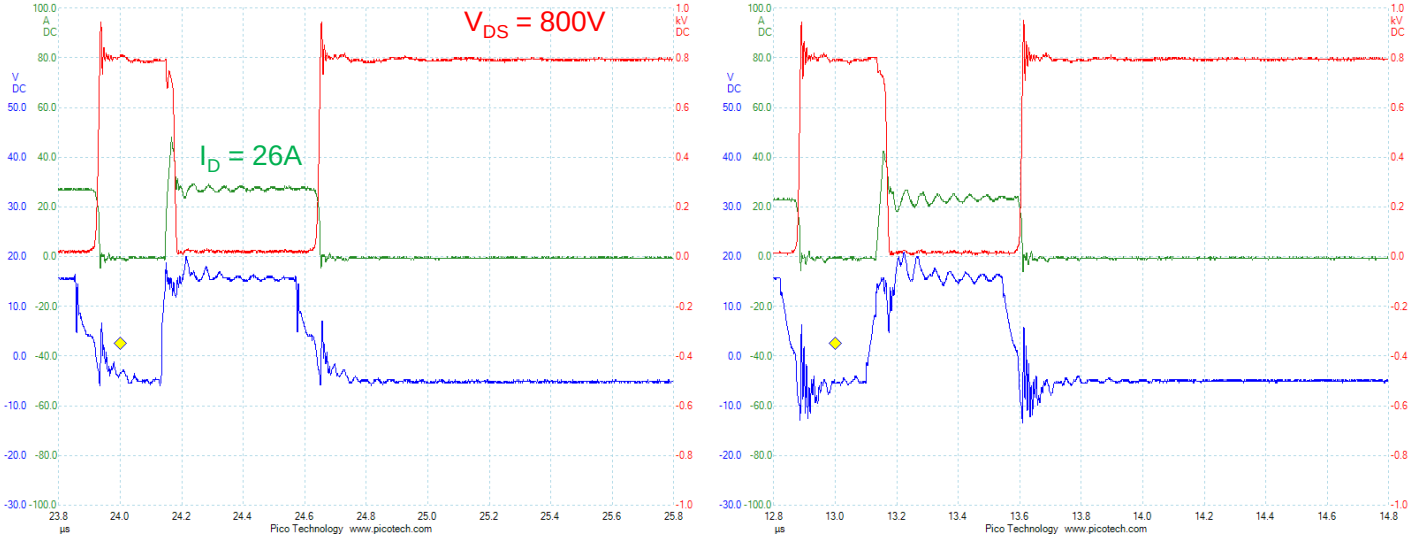
Customer Part Number	MURATA Part Number	Impedance (Ω) (at 100MHz, Under Standard Testing Condition)		Rated Current (mA) (*1)		DC Resistance (Ω) max.		Remark
			Typical	at 85°C	at 125°C	Initial Values	Values After Testing	
	BLM41PG600SN1L	30 min.	60	*1 6000	*1 3700	0.009	0.018	For DC power line
	BLM41PG600SN1B							
	BLM41PG750SN1L	45 min.	75	*1 3500	*1 2450	0.015	0.03	
	BLM41PG750SN1B							
	BLM41PG181SN1L	180±25%	180	*1 3500	*1 2100	0.02	0.04	
	BLM41PG181SN1B							
	BLM41PG471SN1L	470±25%	470	*1 2000	*1 1350	0.05	0.10	
	BLM41PG471SN1B							
	BLM41PG102SN1L	1000±25%	1000	*1 1500	*1 1000	0.09	0.18	
	BLM41PG102SN1B							

• Operating Temperature: -55°C to +125°C • Storage Temperature: -55°C to +125°C



- Ferrite beads may be use to control gate ringing.
- Smaller Rgoff values can be used with beads to reduce delay times, and reduce Eoff.

Comparison of Switching Waveforms with and without using Ferrite Bead (Tj = 125°C, 800V-26A)



Ferrite beads not used:

- Switch Rgon=1Ω, Rgoff = 20Ω, Vgs = -5V to 15V
- FWD: Rgoff = 20Ω, Vgs = -5V

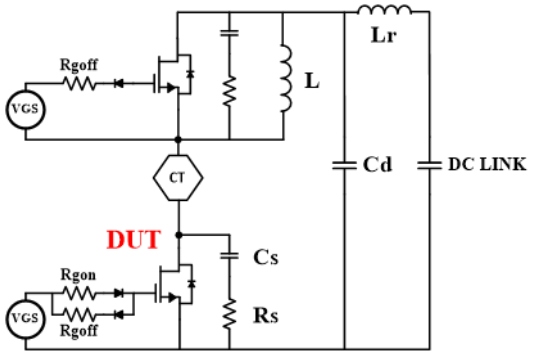
Ferrite beads used:

- Switch Rg=3.3Ω, Vgs = -5V to 15V
- FWD: Rg = 3.9Ω, Vgs = -5V

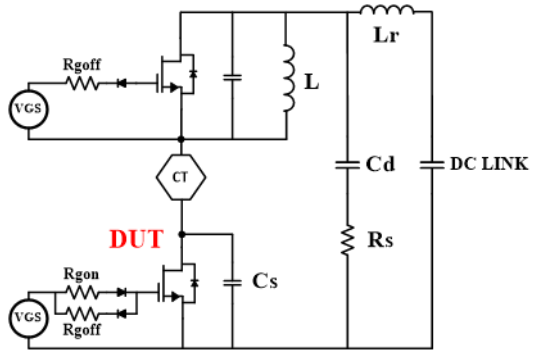
Using a ferrite bead, Turn-on peak current is lower with the bead since di/dt is reduced. Since lower Rg can be used with a ferrite bead, turn-off and turn-on delay times can be minimized.

Using Snubbers to manage switching waveforms

- UnitedSiC FETs have low C_{OSS}
- Snubber capacitances needed are 1 to 3X of C_{OSS}
- Therefore, very small snubber capacitances are needed to control voltage overshoot and reduce current ringing
- The net loss impact is 1-5% of E_{ON} + E_{OFF}
- Small surface mount components are usable, since Snubber R_S loss is between 0.25W to 2W , depending on frequency (while switching 50A, 800V).

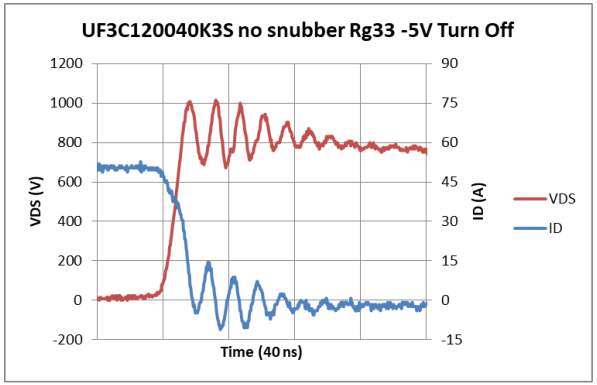


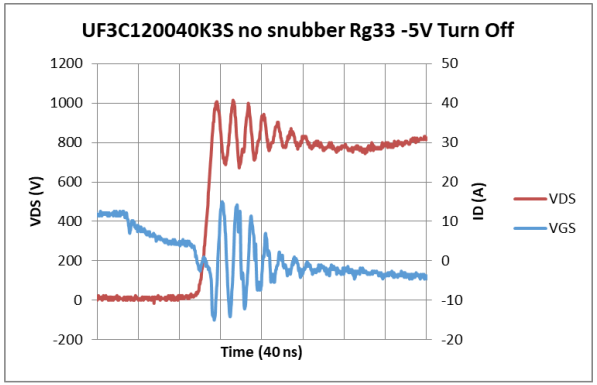
Hard Switching: Basic RC snubber

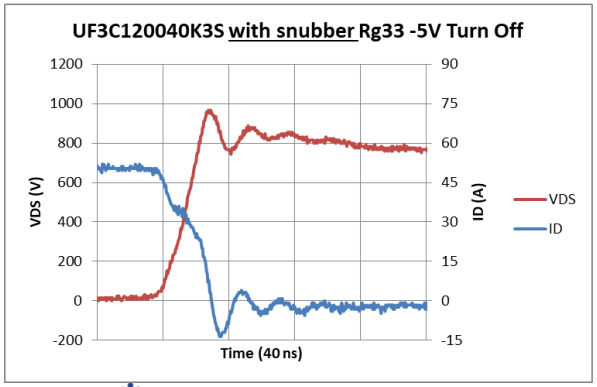


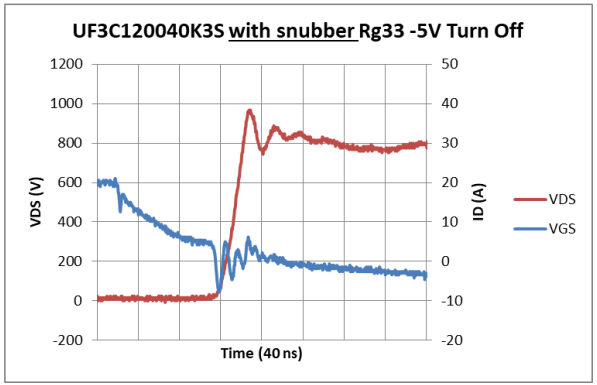
ZVS: RC snubber in series with de-coupling capacitor

Snubber Design for UF3C120040K3S









- Cascode turn-off ringing may be reduced by high $R_{G,OFF}$ but this leads to long delay times
- Waveforms in the second row show how the V_{DS} and V_{GS} ringing are dramatically improved with a small snubber, switching the FETs at 50A, 800V.
- Snubber loss is <2.5% of total E_{ON}+E_{OFF} at 10A and < 1.5% at 50A.

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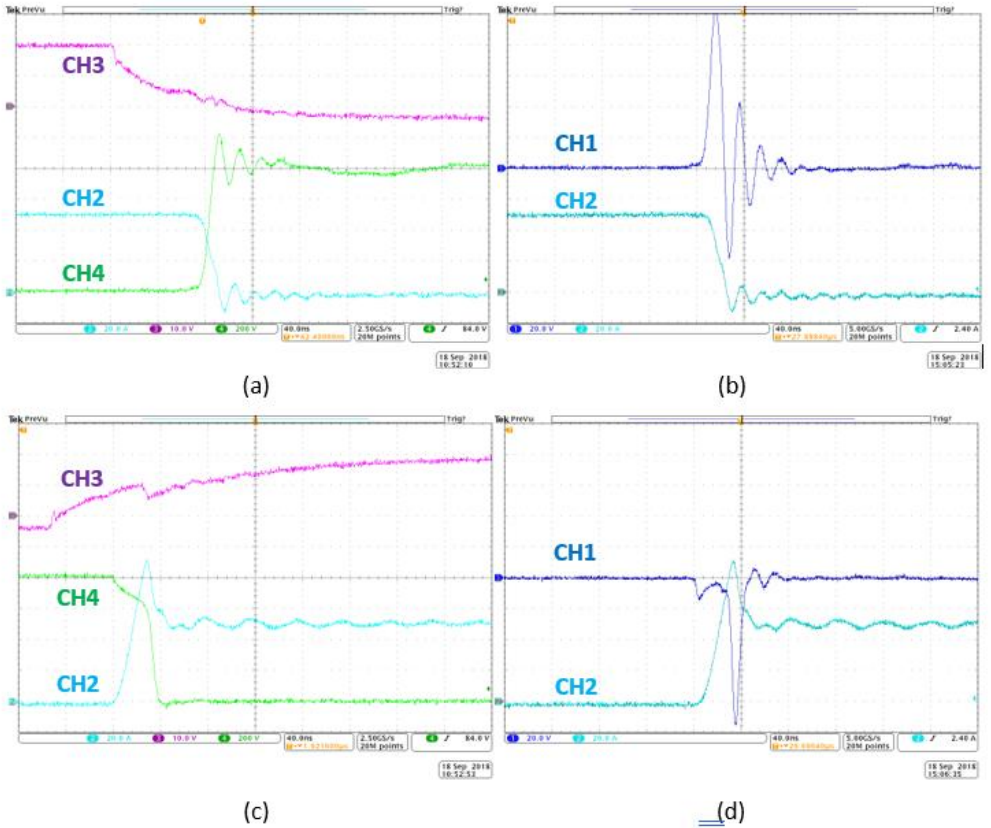
Measuring snubber resistor loss

UF3C120040K4S HALF_BRIDGE

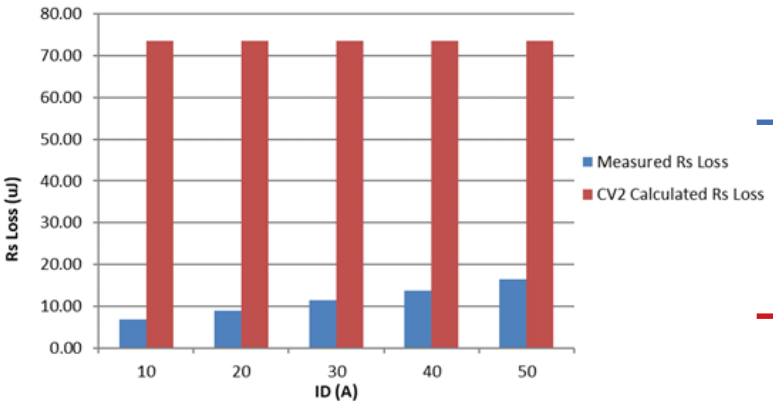
VDS 800V, ID 50A, 125°C, VGS 20V/-5V,
Rgon 50Ω, Rgoff 33Ω,
Snubber Cs 115pF, snubber Rs 10Ω

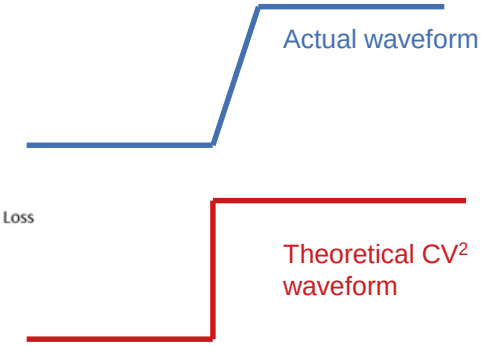
CH1: Snubber Rs voltage (20V/div);
CH2: Drain current (20A/div);
CH3: VGS (10V/div);
CH4: VDS (200V/div).

(a) Turn-off waveforms
(b) Snubber Rs voltage at turn-off CH1
(c) Turn-on waveforms
(d) Snubber Rs voltage at turn-on CH1



Snubber loss measured





ID(A)	ESW(uJ)	ESNUB(uJ)	Ratio
10	494.8	6.86	1.39%
20	642.1	8.85	1.38%
30	811.1	11.39	1.40%
40	981.6	13.69	1.39%
50	1186.5	16.45	1.39%

10ohm, 115pF, 800V
UF3C120040K4S

UF3C120040K4S snubber Rs loss measurement vs. conventional CV^2 calculation.

This occurs because the CV^2 method assumes a constant charging voltage (infinite dV/dt), whereas practically, the device dV/dt regulates the maximum charging rate

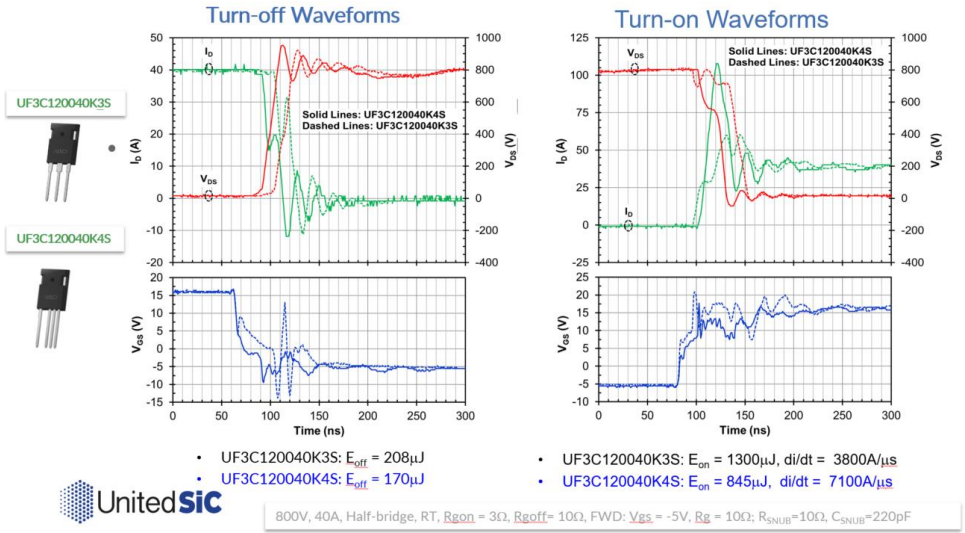
Benefits of Kelvin packages

- Switch faster by overcoming common source inductance
- Cleaner gate waveforms, even with much faster di/dt

DFN8X8

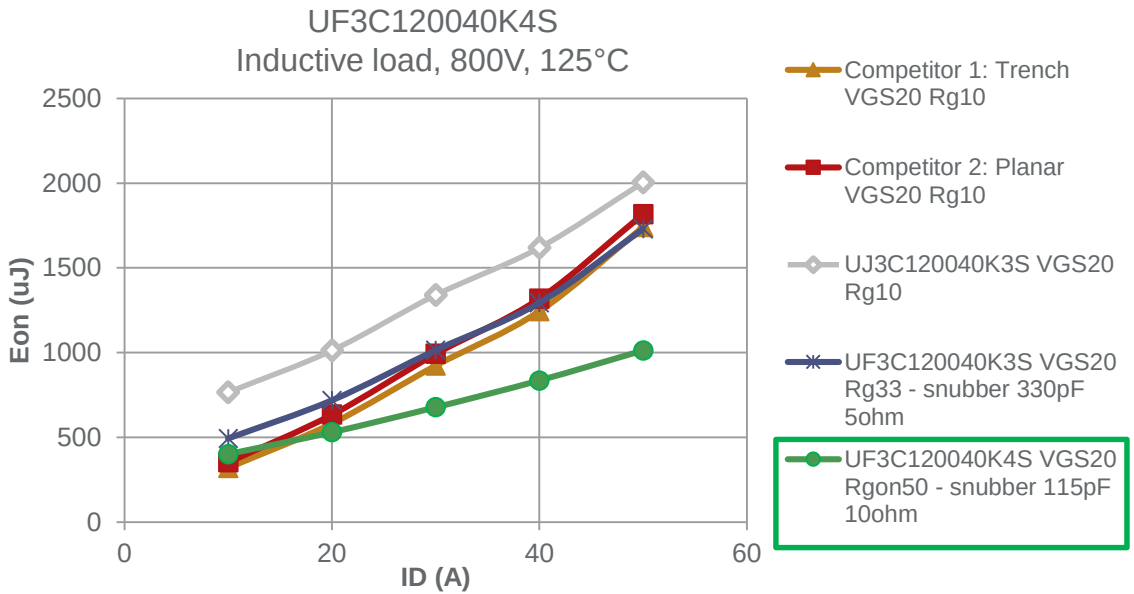
D2PAK-7L

TO247-4L



Reduced Turn-on losses (E_{on})

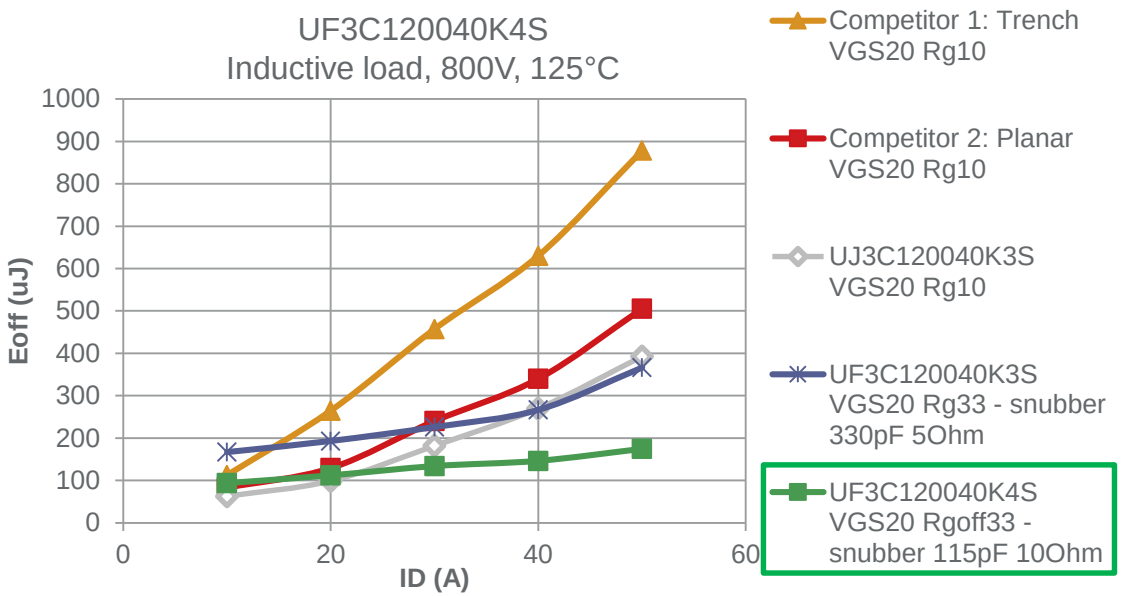
Hard switched half-bridge



- *Dramatic improvement in E_{on} at higher current levels*
- *Snubber loss included*

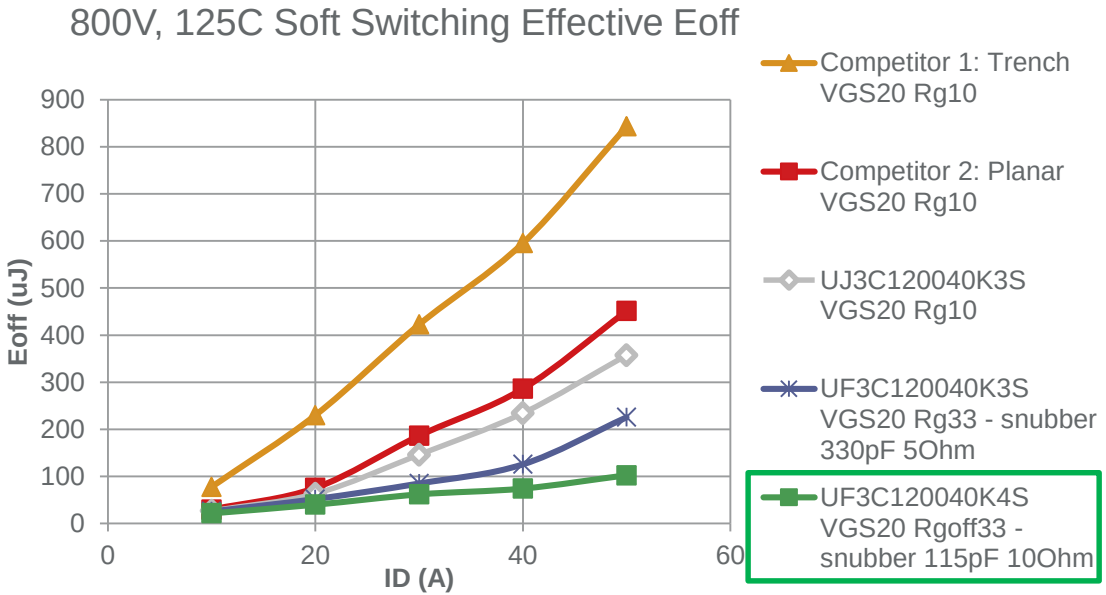
Reduced Turn-off losses (E_{off})

Hard switched half-bridge



- *Very low Eoff losses even at 50A*
- *Snubber loss included*

Excellent choice in soft switched circuits too



Effective turn-off loss ≈

E_{off} (HS) - (E_{oss} + E_{cs})

New SiC FET User Guide

- ✓ Device selector by spec
- ✓ RC snubber guide
- ✓ End application device selection

650V FETs

									Gate Drive voltage positive rail RGON				Gate Drive voltage negative rail RGOFF								Hard switched applications. Active rectifier, Totem Pole PFC, Full-bridge etc.			ZVS applications LLC		ZVS applications PSFB	
Product Name	Package	Vdsmax	Id (25C)	Id (100C)	RthjC (Typ)	Rds(25C)	Rds(125C)	Rds(175C)	10V	12V	15V	20V	0V	-5V	RC snubber	Rsnub	Csnub	Esnub @10A	Esnub @30A	Coss(er)	Upto 20kHz	20-100KHz	>100kHz	50-150kHz	150-500kHz	20-50kHz	50-200kHz
Units		**V**	**A**	**A**	**C/W**	**mΩ**	**mΩ**	**mΩ**	**Ω**	**Ω**	**Ω**	**Ω**	**Ω**	**Ω**		**Ω**	**pF**	**uJ**	**uJ**	**pF**							
UJ3C065080T3S	TO220-3L	650	31	23	0.61	80	110	140	5	10	20	30	5	10	Optional	4.7	220				X			X		X	
UJ3C065080K3S	TO247-3L	650	31	23	0.61	80	110	140	5	10	20	30	5	10	Optional	4.7	220				X			X		X	
UJ3C065080B3	D2PAK-3L	650	25	18.2	1	80	110	140	5	10	20	30	5	10	Optional	4.7	220				X			X		X	
UF3C065080T3S	TO220-3L	650	31	23	0.61	80	110	140	5	10	20	30	10	20	Required	4.7	220					X					
UF3C065080K3S	TO247-3L	650	31	23	0.61	80	110	140	5	10	20	30	10	20	Required	4.7	220			77		X					
UF3C065080B3	D2PAK-3L	650	25	18.2	1	80	110	140	5	10	20	30	10	20	Required	4.7	220					X					
UF3C065080B7S	D2PAK-7L	650	TBD	TBD	TBD	80	110	140	15	20	30	50	5	10	Recommended	10	115					X	X		X	X	X
UF3C065080K4S	TO247-4L	650	31	23	0.61	80	110	140	15	20	30	50	5	10	Recommended	10	115					X	X		X	X	X
UF3C065040T3S	TO220-3L	650	54	40	0.35	42	58	78	5	10	20	30	10	20	Required	4.7	330					X				X	X
UF3C065040K3S	TO247-3L	650	54	40	0.35	42	58	70	5	10	20	30	10	20	Required	4.7	330	16.0	23.0			X				X	X
UF3C065040B3	D2PAK-3L	650	41	30	0.65	42	58	70	5	10	20	30	10	20	Required	4.7	330			150		X				X	X
UF3SC065040B7S	D2PAK-7L	650	TBD	TBD	TBD	42	58	70	15	20	30	50	5	10	Recommended	10	110					X	X		X	X	X
UF3C065040K4S	TO247-4L	650	54	40	0.35	42	58	70	15	20	30	50	5	10	Recommended	10	110					X	X		X	X	X
UF3SC065040D8	DFN88	650	TBD	TBD	TBD	42	58	70	15	20	30	50	5	10	Recommended	10	110					X	X		X	X	X
UJ3C065030T3S	TO220-3L	650	85	62	0.26	27	35	43	5	10	20	50	5	10	Optional	4.7	680				X			X		X	
UJ3C065030K3S	TO247-3L	650	85	62	0.26	27	35	43	5	10	20	50	5	10	Optional	4.7	680	13.8	20.3		X			X		X	
UJ3C065030B3	D2PAK-3L	650	66	47	0.48	27	35	43	5	10	20	50	5	10	Optional	4.7	680				X			X		X	
UF3C065030T3S	TO220-3L	650	85	62	0.26	30	39	48	5	10	20	30	10	20	Required	4.7	680					X				X	X
UF3C065030K3S	TO247-3L	650	85	62	0.26	30	39	48	5	10	20	30	10	20	Required	4.7	680	15.8	22.5			X				X	X
UF3C065030B3	D2PAK-3L	650	66	47	0.48	30	39	48	5	10	20	30	10	20	Required	4.7	680			230		X				X	X
UF3SC065030B7S	D2PAK-7L	650	TBD	TBD	TBD	30	39	48	15	20	30	50	5	10	Recommended	10	220					X	X		X	X	X
UF3C065030K4S	TO247-4L	650	85	62	0.26	30	39	48	15	20	30	50	5	10	Recommended	10	220					X	X		X	X	X
UF3SC065030D8	DFN88	650	TBD	TBD	TBD	30	39	48	15	20	30	50	5	10	Recommended	10	220					X	X		X	X	X

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New SiC FET User Guide

1200V FETs

- ✓ Device selector by spec
- ✓ RC snubber guide
- ✓ End application device selection

									Gate Drive voltage positive rail RGON				Gate Drive voltage negative rail RGOFF								Hard switched applications. Active rectifier, Totem Pole PFC, Full-bridge etc.			ZVS applications LLC		ZVS applications PSFB	
Product Name	Package	Vdsmax	Id (25C)	Id (100C)	RthjC (Typ)	Rds(25C)	Rds(125C)	Rds(175C)	10V	12V	15V	20V	0V	-5V	RC snubber	Rsnub	Csnub	Esnub @10A	Esnub @30A	Coss(er)	Upto 20kHz	20-100kHz	>100kHz	50-150kHz	150-500kHz	20-50kHz	50-200kHz
Units		**V**	**A**	**A**	**C/W**	**mΩ**	**mΩ**	**mΩ**	**Ω**	**Ω**	**Ω**	**Ω**	**Ω**	**Ω**		**Ω**	**pF**	**uJ**	**uJ**	**pF**							
UJ3C120150K3S	TO247-3L	1200	18.4	13.8	0.7	150	255	330	5	10	20	30	5	10	Optional	4.7	100			34	X			X		X	
UF3C120150K3S	TO247-3L	1200	18.4	13.8	0.7	150	255	330	5	10	20	30	10	20	Required	4.7	100					X					
UF3C120150B7S	D2PAK-7L	1200	TBD	TBD	TBD	150	255	330	15	20	30	50	5	10	Recommended	10	47					X	X		X	X	X
UF3C120150K4S	TO247-4L	1200	18.4	13.8	0.7	150	255	330	15	20	30	50	5	10	Recommended	10	47					X	X		X	X	X
UJ3C120080K3S	TO247-3L	1200	33	24	0.45	80	136	172	5	10	20	30	5	10	Optional	4.7	150	5.0	8.0	59	X			X		X	
UF3C120080K3S	TO247-3L	1200	33	24	0.45	80	136	172	5	10	20	30	10	20	Required	4.7	150					X					
UF3C120080B7S	D2PAK-7L	1200	TBD	TBD	0.6	80	136	172	15	20	30	50	5	10	Recommended	10	68					X	X		X	X	X
UF3C120080K4S	TO247-4L	1200	33	24	0.45	80	136	172	15	20	30	50	5	10	Recommended	10	68					X	X		X	X	X
UJ3C120040K3S	TO247-3L	1200	65	47	0.27	35	56	73	5	10	20	30	5	10	Optional	4.7	330	14.7	21.6	112	X			X		X	
UF3C120040K3S	TO247-3L	1200	65	47	0.27	35	56	73	5	10	20	30	10	20	Required	4.7	330	16.1	23.5			X					
UFS3C120040B7S	D2PAK-7L	1200	TBD	TBD	TBD	35	56	73	15	20	30	50	5	10	Recommended	10	110	6.9	11.4			X	X		X	X	X
UF3C120040K4S	TO247-4L	1200	65	47	0.27	35	56	73	15	20	30	50	5	10	Recommended	10	110					X	X		X	X	X

Cs (pF)	Series	Part Number	Package	Rated V
47	C0G	202R18N470JV4E	1206	2000V
68		C1206C680JGGAC7800	1206	2000V
100		202R18N101JV4E	1206	2000V
150		C1206C151JGGAC7800	1206	2000V
220		C1206C221JGGAC7800	1206	2000V
330		C1210C331JGGACTU	1210	2000V
680		C1808C681JGGAC7800	1808	2000V

"C0G" ceramic capacitors are most stable.

Rs (Ω)	Power Rating (W)	Part Number	Package
4.7	0.25	KTR18EZPF4R70	1206
	0.5	SR1206FR-7W4R7L	1206
	1	CRCW20104R70JNEFHP	2010
	1.5	CRCW25124R70JNEGHP	2512
10	0.25	KTR18EZPF10R0	1206
	0.5	SR1206FR-7W10RL	1206
	1	CRCW201010R0JNEFHP	2010
	1.5	CRCW251210R0JNEGHP	2512

For "KTR18" resistor is rated at 500V and the overload voltage is 1000V.

For "SR1206" resistor is rated at 200V, the overload voltage is 400V, the dielectric withstanding voltage is 500V.

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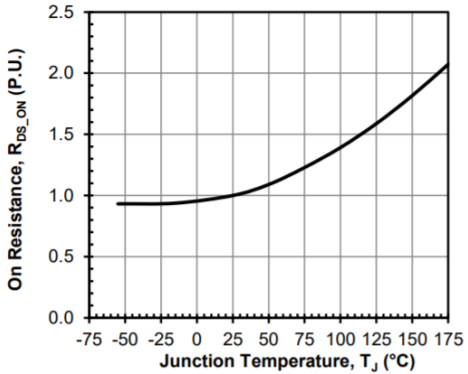
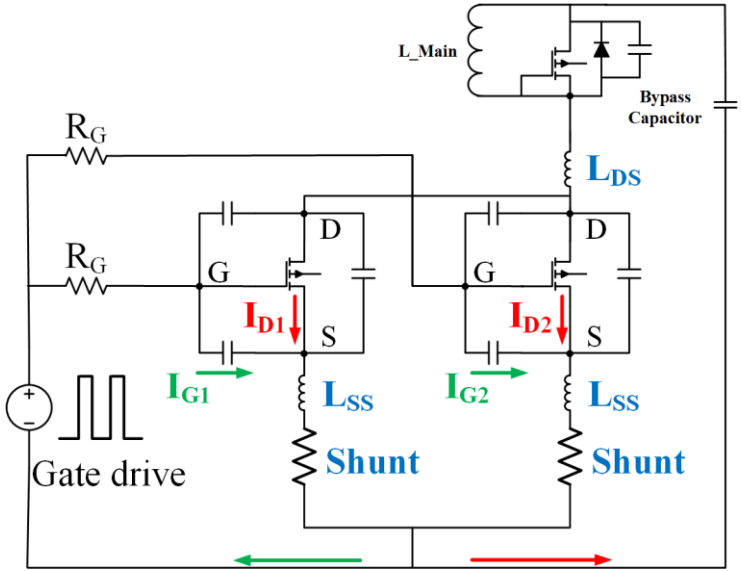
Paralleling discrete devices for higher power

GENERAL GUIDELINES FOR PCB LAYOUT

- Symmetry
- Minimum PCB stray inductances
- Separate gate resistor
- Minimize capacitive coupling between gate and drain of each transistor.



Rds positive temperature coefficient aids current sharing



L_{DS}: main loop stray inductance
L_{SS}: common source inductance

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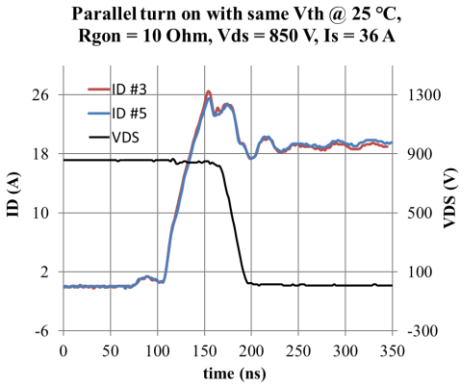
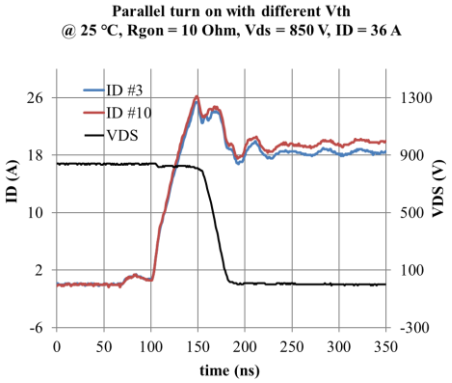
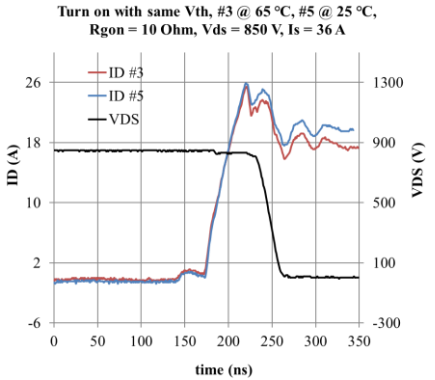
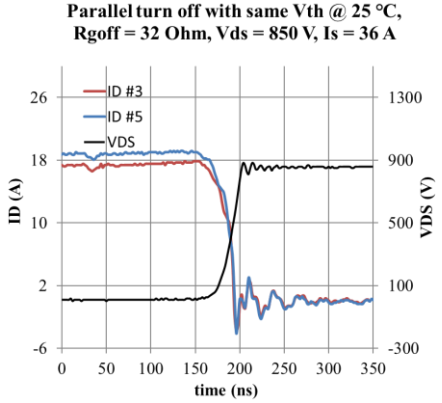
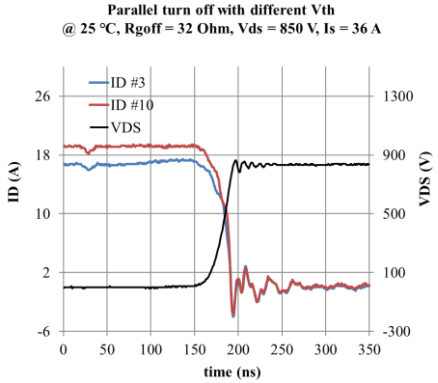
Paralleling discrete devices for higher power

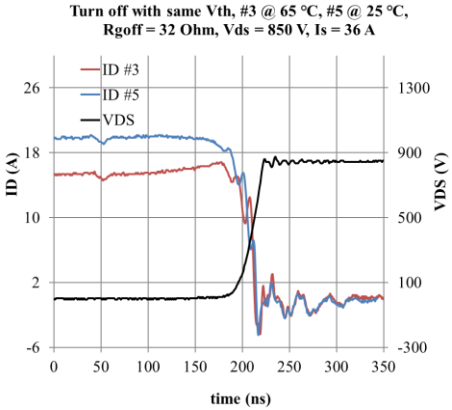












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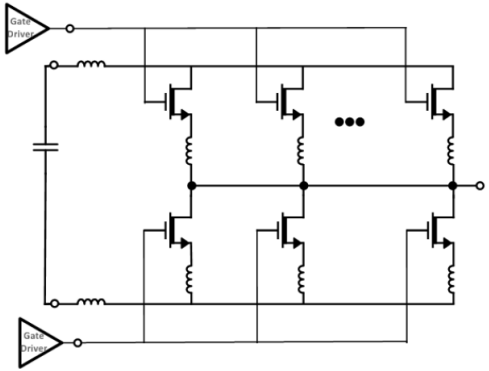
Vth mismatch

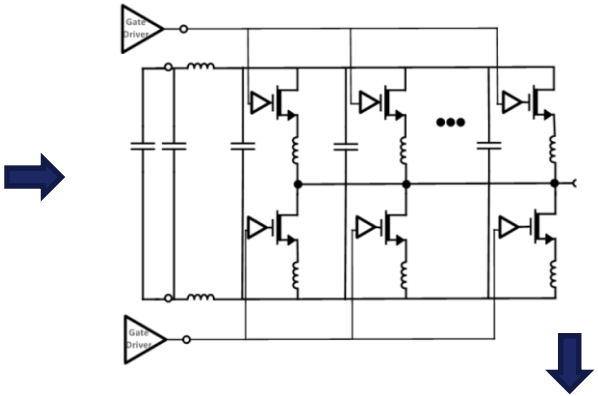
T_J mismatch of 40C

UnitedSiC FET paralleling is tolerant of typical parametric mismatches and temperature differentials

Scalable SiC Cascode Power Blocks

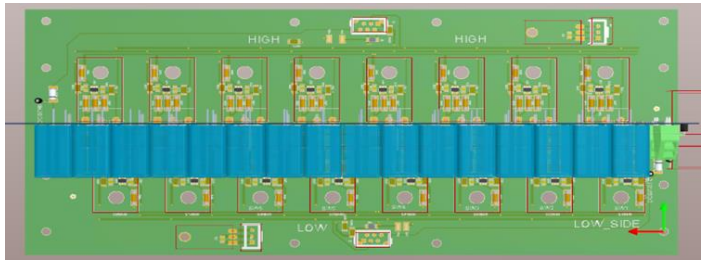
Conventional Method:
Single external gate driver and capacitor at module level => All circuit legs switch through common parasitic inductance.

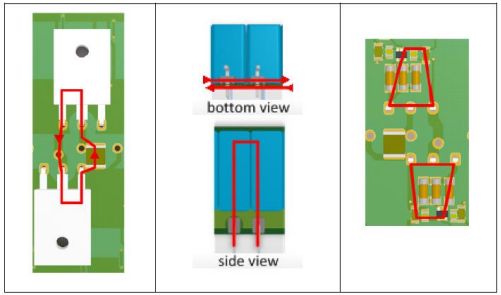




Preferred Method:
Local bus capacitance and gate drive buffer for each circuit leg => High frequency switching contained within each converter leg.

Layout of 8 Parallel Legs





Power loop showing the Bottom of the PCB, the central “bus bar”, and the gate drive loops on the Top layer

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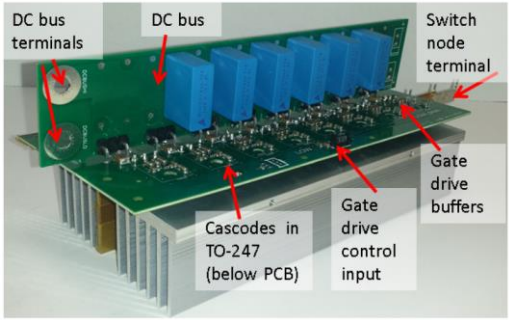
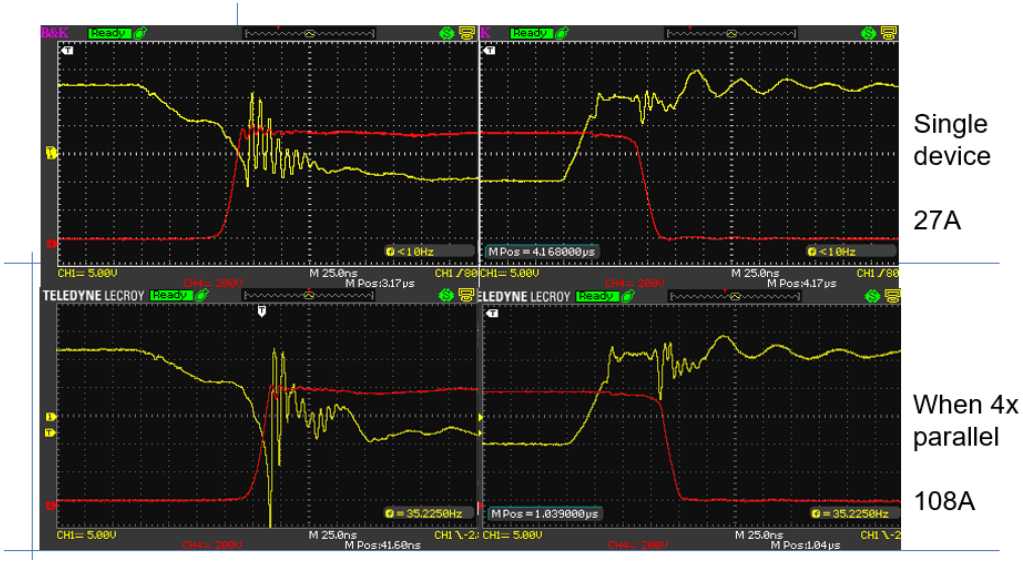
Scalable SiC Cascode Power Blocks



Power blocks have been built for half-bridges and TNPC units with upto 8X units in parallel



Switching of a power block with 4X HS and 4X LS SiC FETs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APPENDIX

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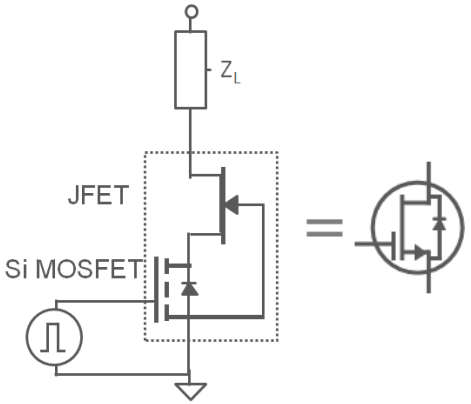
How the cascode FET works

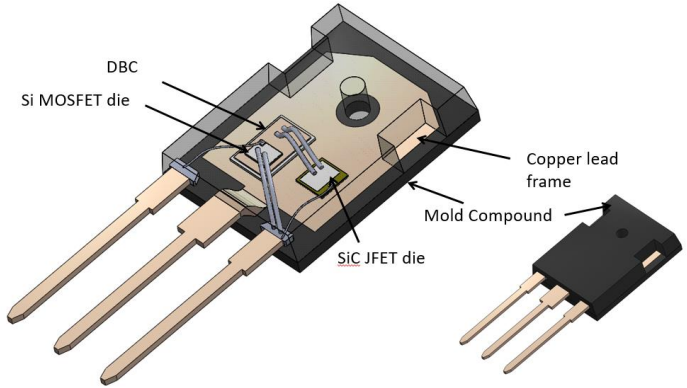


Cascode Internal Operation

JFET V_{GS} = - MOSFET V_{DS}

Turn On
- MOSFET turns "On"
  - MOSFET V_{GS} > MOSFET V_{TH}
  - MOSFET V_{DS} ~ 0 V
- JFET turns "On"
  - MOSFET V_{DS} ~ 0, JFET V_{GS} ~ 0 V
    - JFET V_{TH} is -6 V typical

Turn Off
- MOSFET turns "Off"
  - MOSFET V_{GS} < MOSFET V_{TH}
  - MOSFET "Off", V_{DS} rises > 6 V
- JFET turns "Off"
  - High Voltage Across JFET V_{DS}



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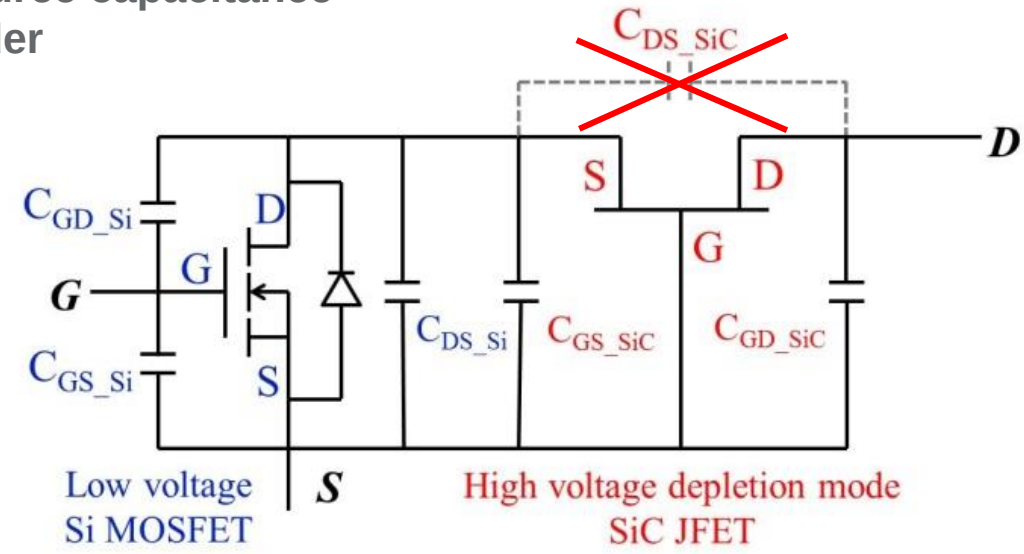
Easy to Cascode JFET Design

- UnitedSiC JFET has zero drain-source capacitance
- No drain-source-gate voltage divider
- Good for ZVS operation
- Stable



Ref: X. Huang, W. Du, F.C. Lee, Q. Li and Z. Liu, “Avoiding Divergent Oscillation of a Cascode GaN Device Under High-Current Turn-Off Condition”, IEEE Trans. Power Electron., 2017

Body Diode V_F: UnitedSiC FET vs SiC MOSFET

Low VF & Qrr eliminates need for separate anti-parallel diode

Typical UnitedSiC FET

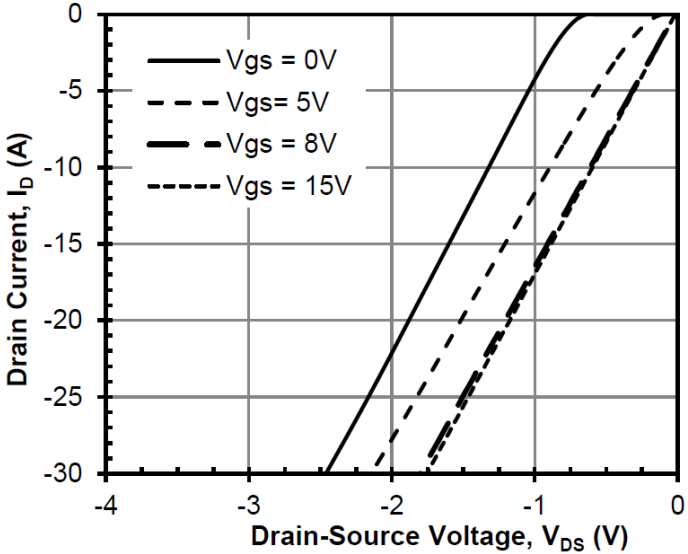


Figure 10 3rd quadrant characteristics at T_J = 25°C

Typical SiC MOSFET

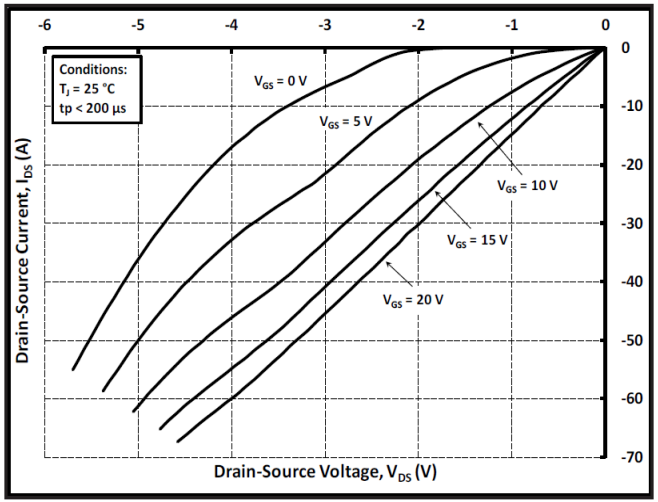


Figure 14. 3rd Quadrant Characteristic at 25 °C

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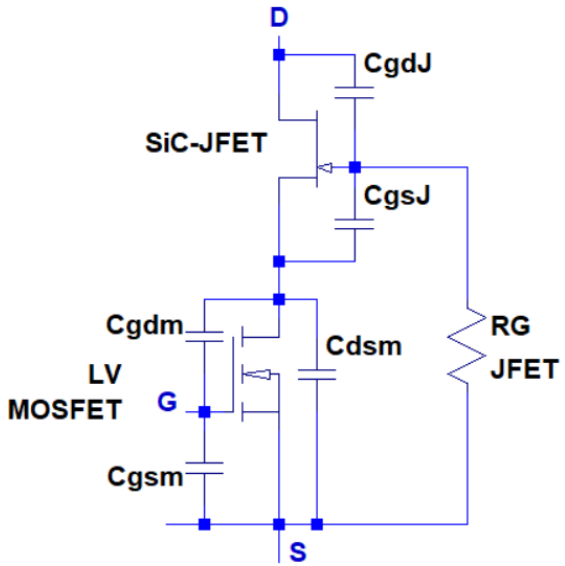
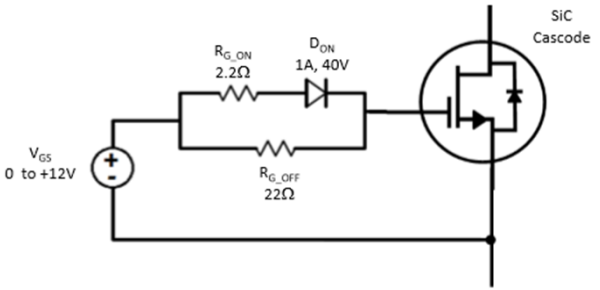
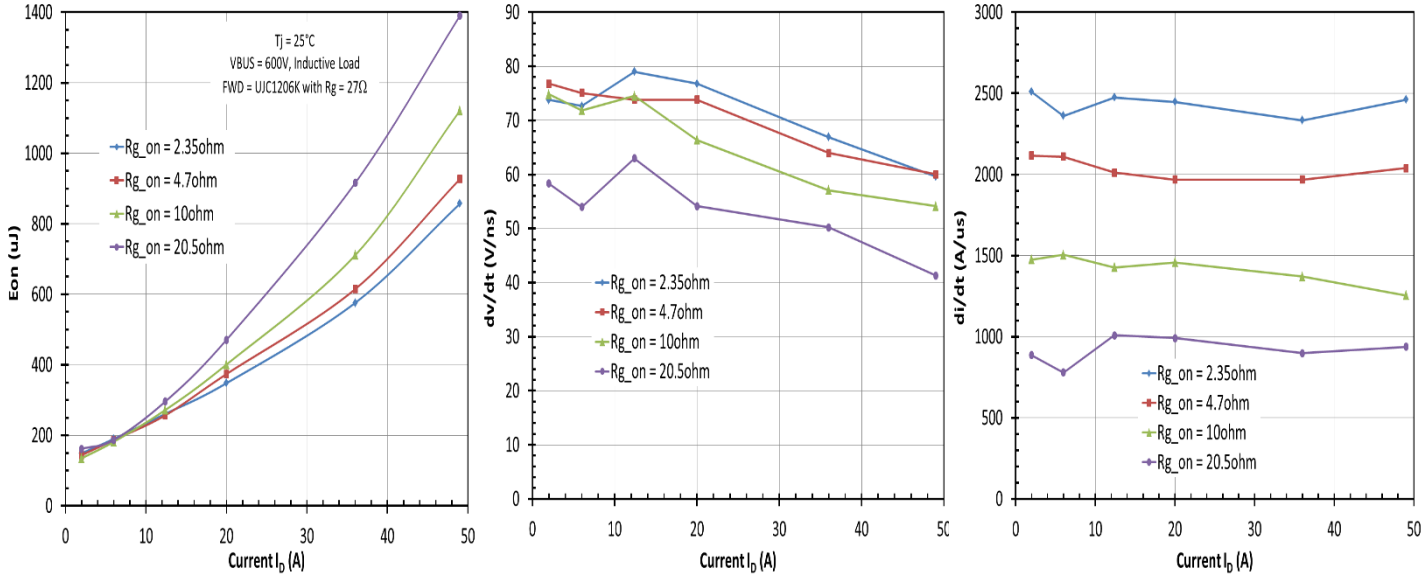
What controls switching speeds

- Turn-on di/dt can be slowed by MOSFET Rgon in a TO247-3L, where L_s de-biases the $V_{gs(MOS)}$. So higher V_{gs} values can speed up di/dt.
- The upper limit to the di/dt is set by the fact that the JFET Vth is fixed, and the JFET experiences a $V_{GS(JFET)}$=-$V_{DS(MOS)}$ that is fixed. The internal inductance and the R_{GJFET}*(C_{gsJ}+$C_{oss(MOS)}$) sets this maximum di/dt.
- Once the MOSFET has turned off enough to pinch-off the JFET, dV/dt is largely regulated by the C_{gdJ}*R_{GJFET}. However, slowing the MOSFET drain node using a external R_{goff} can influence the turn-off rate, essentially slowing the gate voltage applied to the JFET at turn-off.

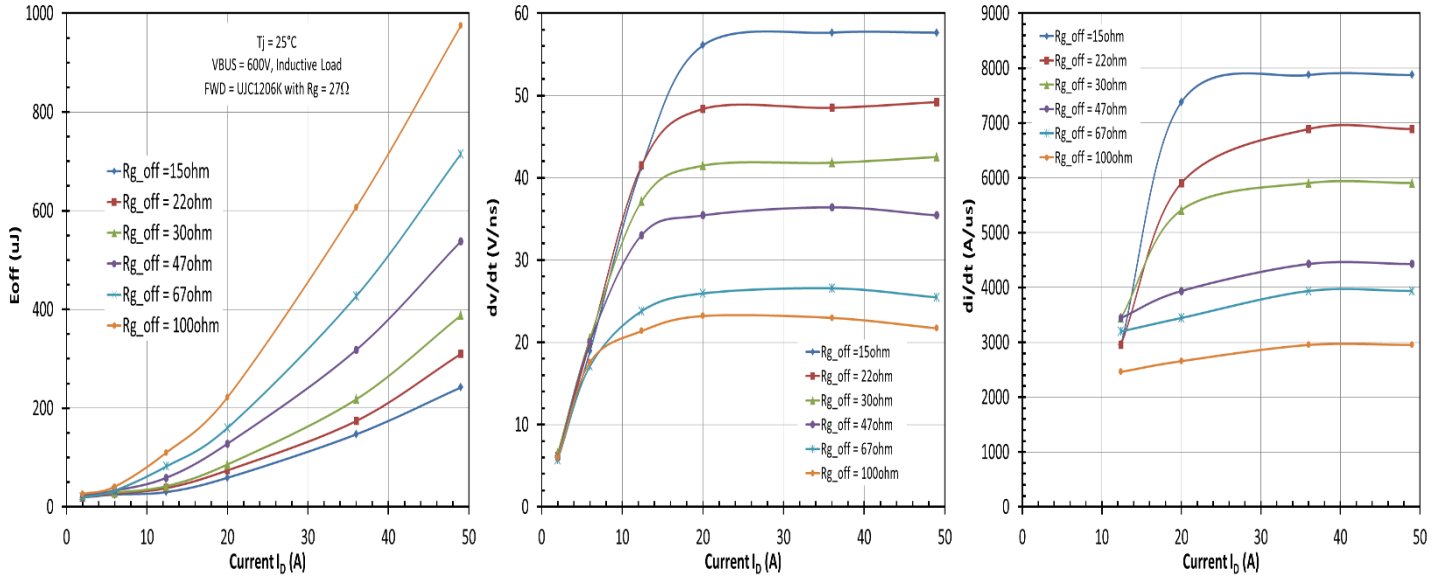




Measured Turn-on Energy Loss, di/dt and dv/dt with 600V Inductive Load. FWD: UJC1206K

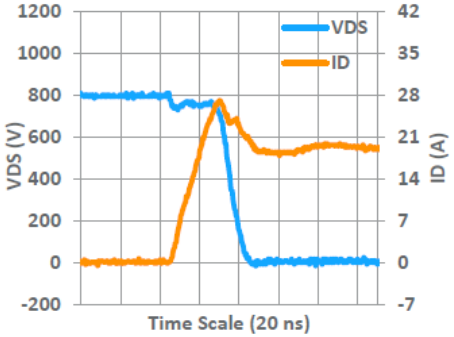


Measured Turn-off Energy Loss, di/dt and dv/dt with 600V Inductive Load Condition. FWD: UJC1206K

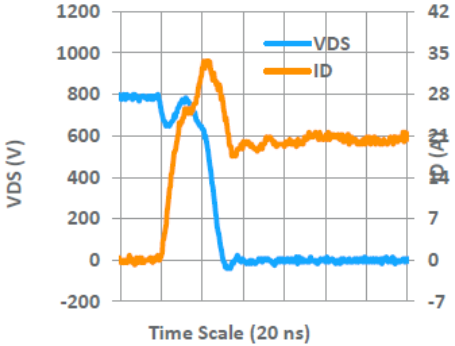


Comparing G2, G3 cascodes and SiC MOSFETs in half-bridge

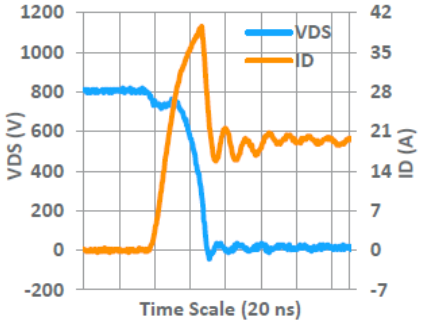
UJC1210K, 12V/-5V
Rgon = 2.3 Ω, Rgoff = 10 Ω, Eon = 406 uJ
didt = 1.28 A/ns, dvdt = 69 V/ns



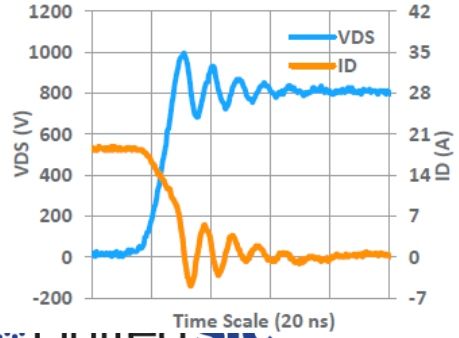
UJ3C120080K3S, 15V/-5V
Rgon = 1 Ω, Rgoff = 20 Ω, Eon = 392 uJ
didt = 2.78 A/ns, dvdt = 78 V/ns



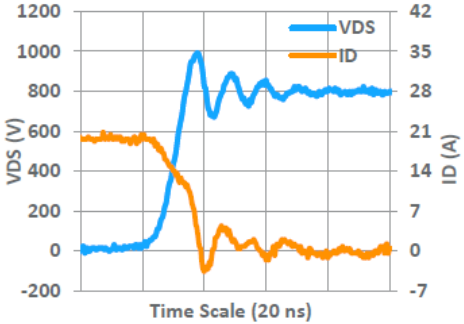
C2M080120D, 18V/-5V
Rgon = 5 Ω, Rgoff = 5 Ω, Eon = 446 uJ
didt = 2.1 A/ns, dvdt = 71 V/ns



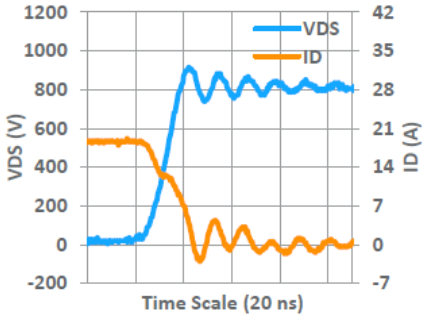
UJC1210K
Rgon = 2.3 Ω, Rgoff = 10 Ω, Eoff = 101 uJ
didt = 4.2 A/ns, dvdt = 86 V/ns



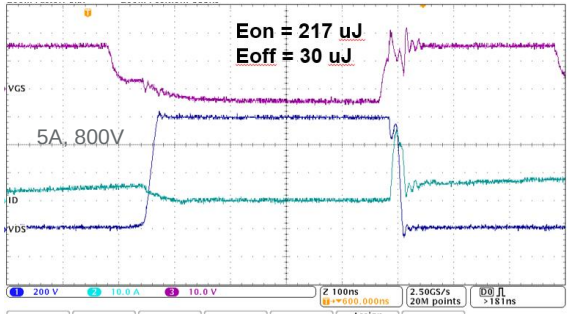
UJ3C120080K3S
Rgon = 1 Ω, Rgoff = 20 Ω, Eon = 107 uJ
didt = 3.7 A/ns, dvdt = 85 V/ns

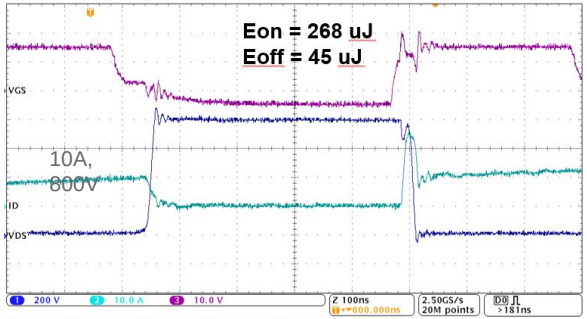


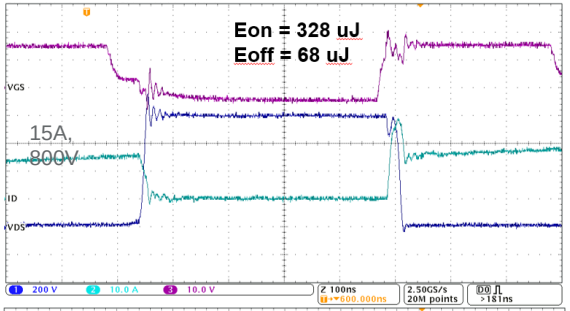
C2M080120D
Rgon = 5 Ω, Rgoff = 5 Ω, Eoff = 115 uJ
didt = 2.3 A/ns, dvdt = 60 V/ns

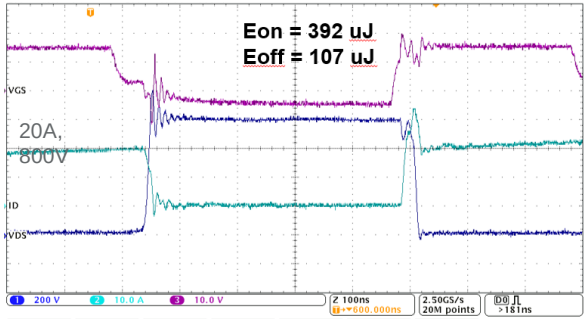


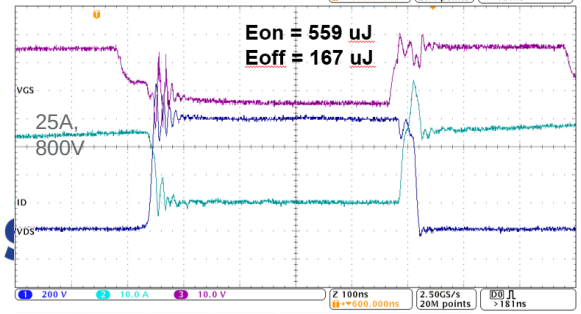
UJ3C120080K3S Half-bridge Vgs drive +15V/-5V
Rgon=1ohm, Rgoff=20ohm, 125C



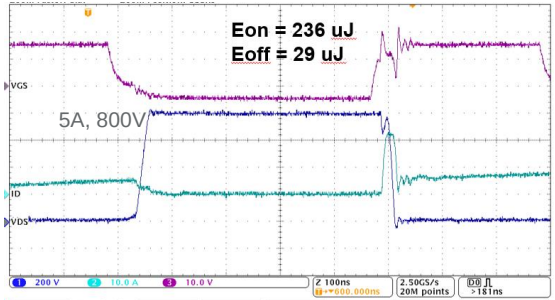


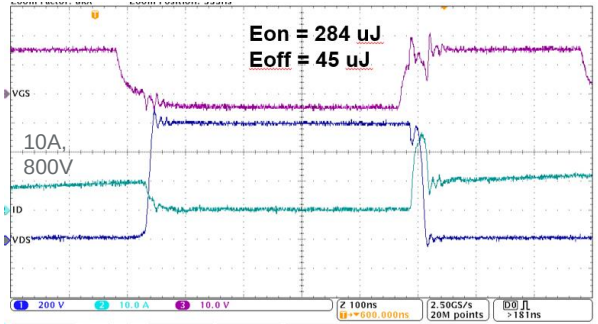


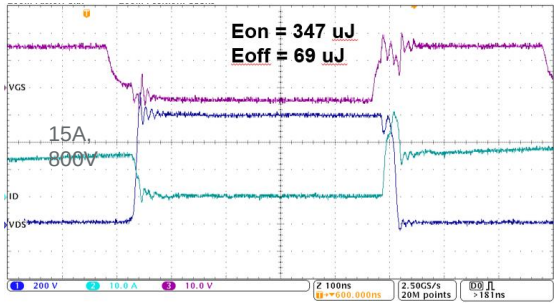


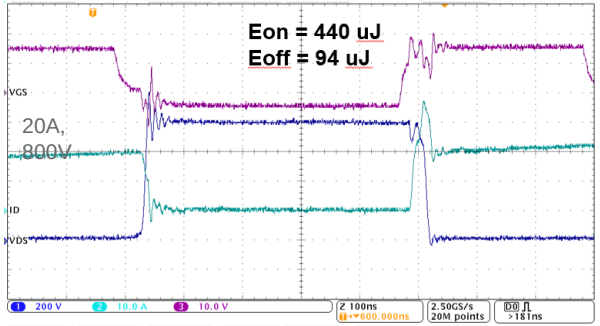


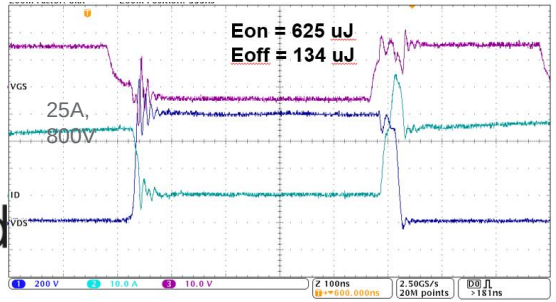
UJ3C120080K3S Half-bridge Vgs drive +15V/-5V Rgon=2.3ohm, Rgoff=8ohm, 125C











UJ3C switching characteristics
80m, 1200V

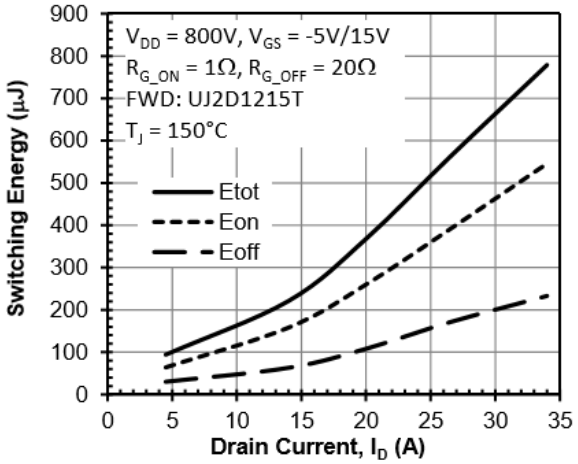


Figure 18 Clamped inductive switching energy vs. drain current at T_J = 150°C

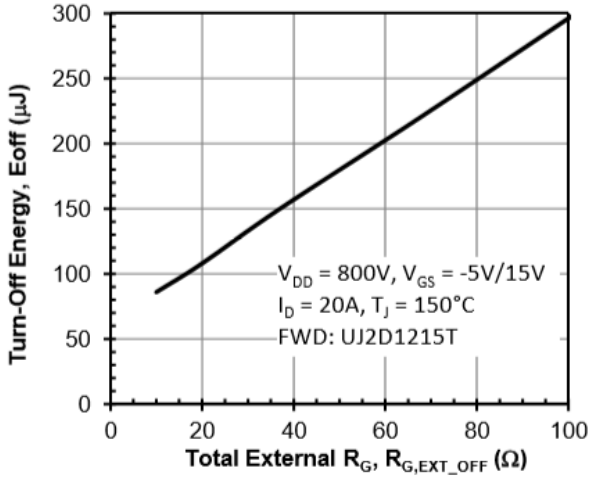


Figure 20 Clamped inductive switching turn-off energy vs. R_{G,EXT_OFF}

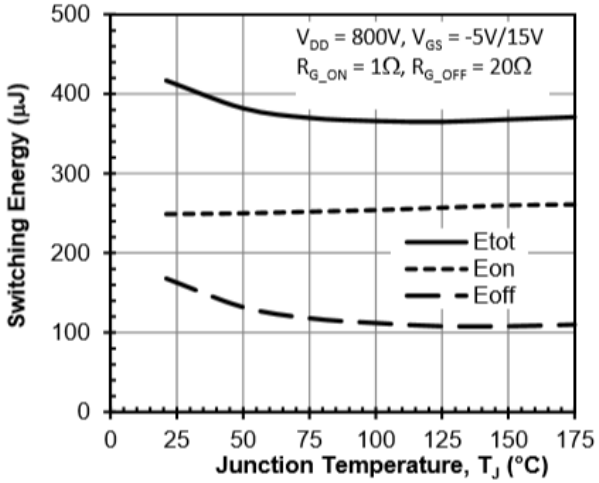


Figure 21 Clamped inductive switching energy vs. junction temperature at I_D = 20A

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UJ3C switching characteristics
30m, 650V

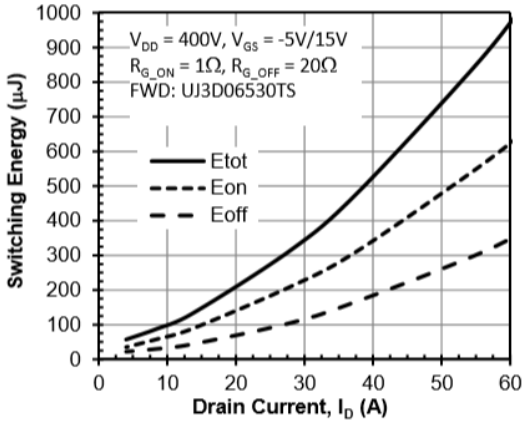

Figure 18 Clamped inductive switching energy vs. drain current at T_J = 150°C

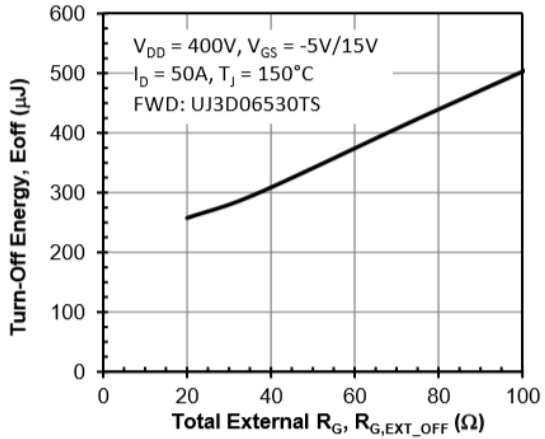

Figure 20 Clamped inductive switching turn-off energy vs. R_{G,EXT_OFF}

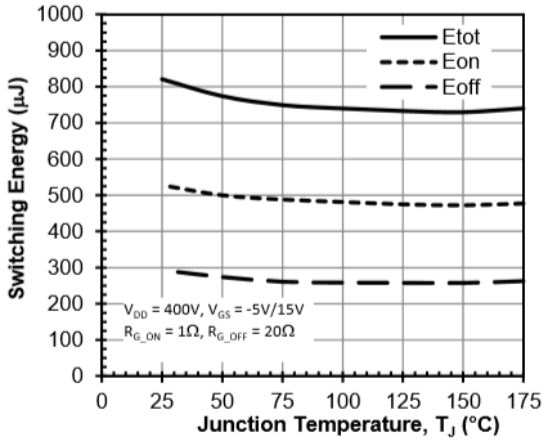

Figure 21 Clamped inductive switching energy vs. junction temperature at I_D = 50A

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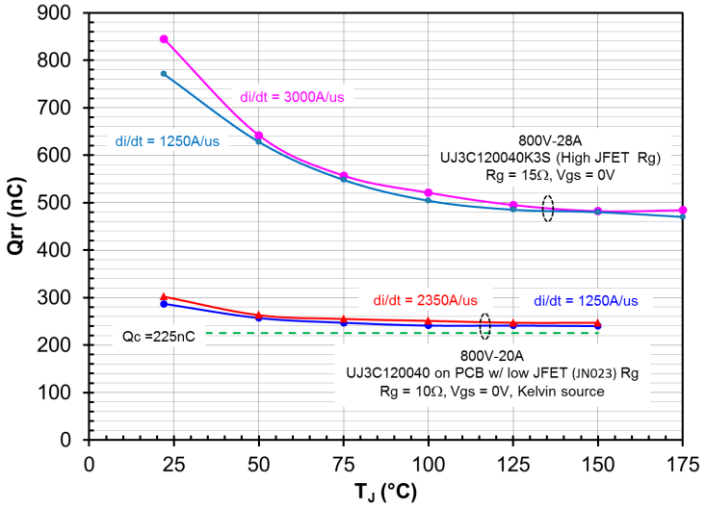
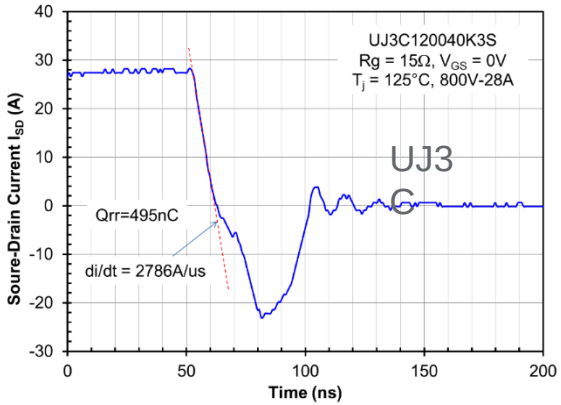
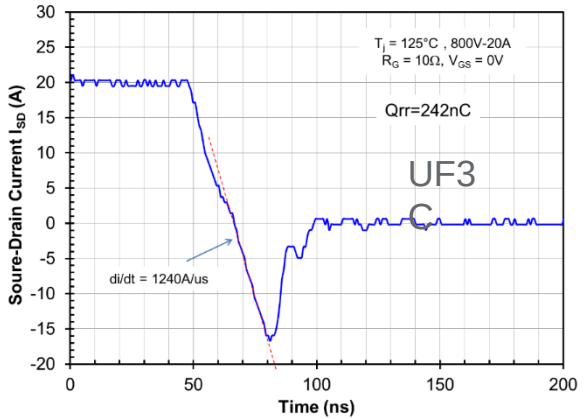
Measured Qrr of UJ3C120040K3S vs UF3C120040K4S

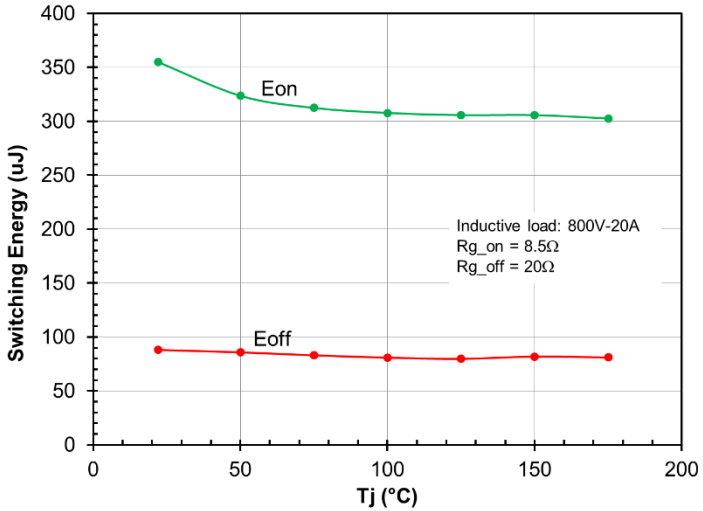


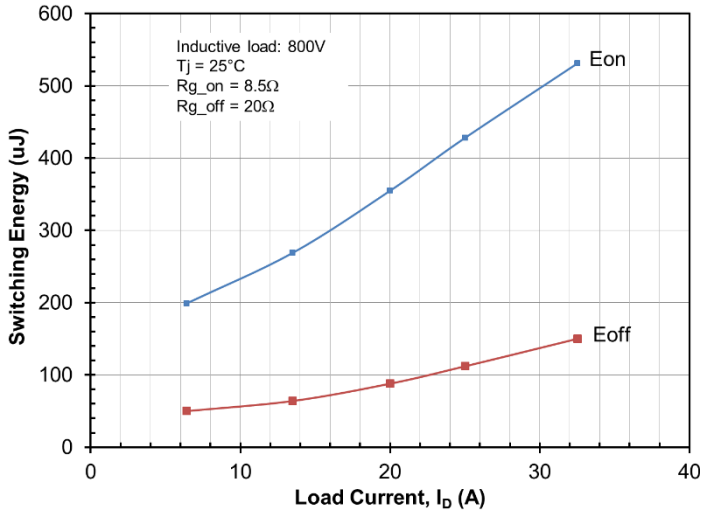




Minimum Qrr in a cascode is Qc, the integrated Coss charge

UF3C120080K4S
Half-Bridge Switching Energies





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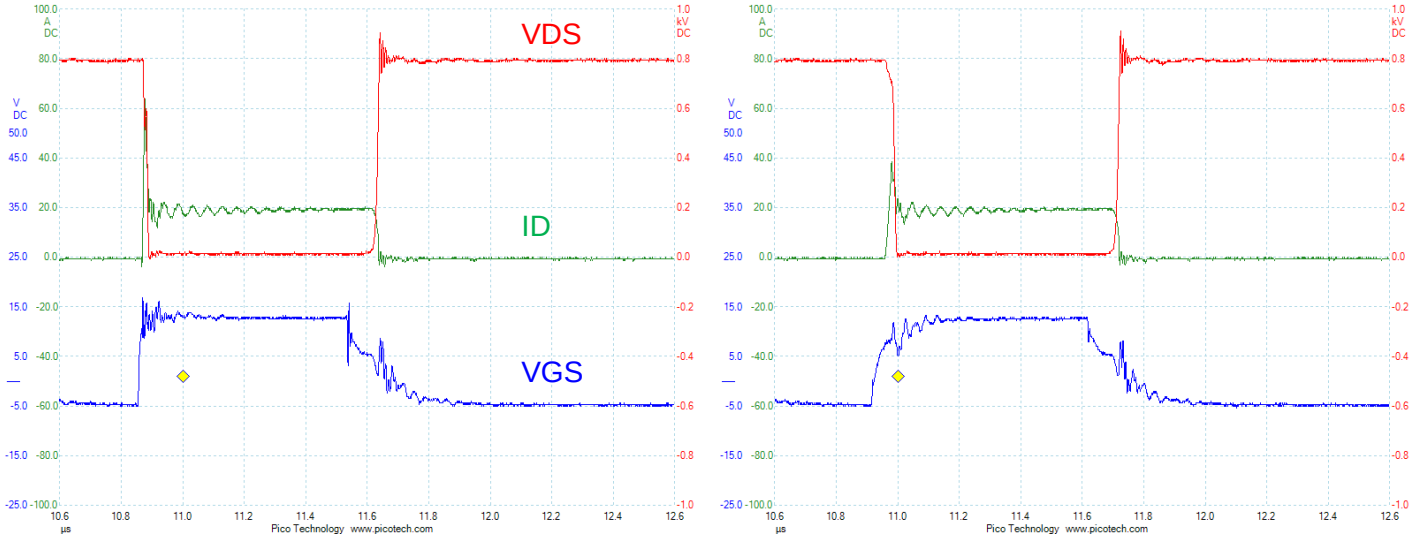
UF3C120080K4S Switching Waveforms
800V, Tj = 25°C, Vgs = -5V/+12V



Rg_on = 1Ω
Rg_off = 47Ω
Turn-on di/dt =8563A/us

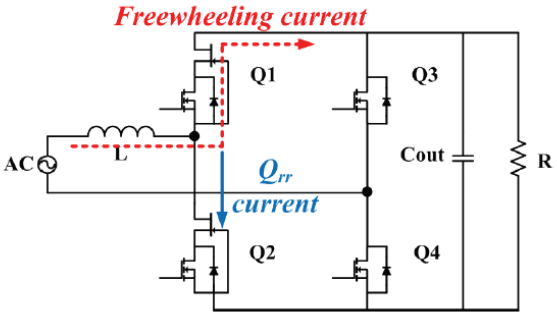
Rg_on = 21Ω
Rg_off = 47Ω
Turn-on di/dt =1995A/us

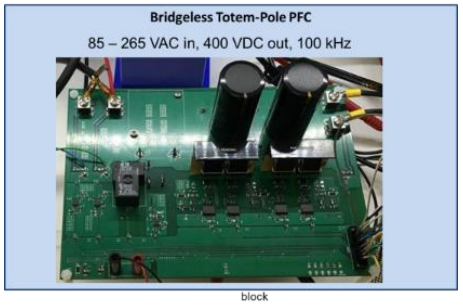
ZVS circuits LLC, PSFB

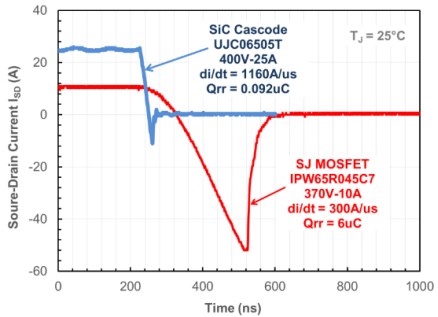
- Since turn-on is no longer critical, it should generally be possible to use a single Rgoff.
- Depending on current 5-20ohm works well
- Sufficient to limit gate drive to 0-12V – no benefit with higher Vgs, no benefit with negative gate drive
- A bead can still be used if currents are high, or if a low Rgoff is required to minimize delay time at high frequencies

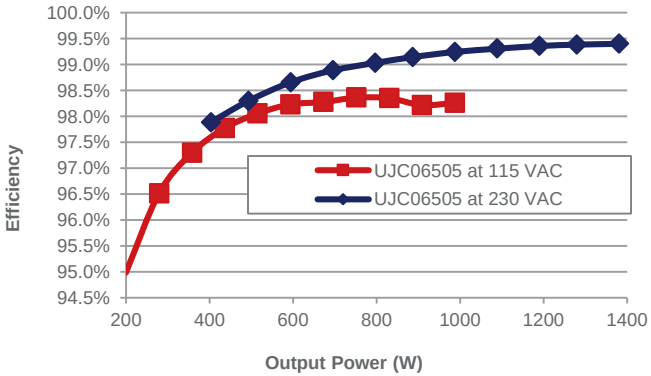
650V cascode – Totem Pole PFC

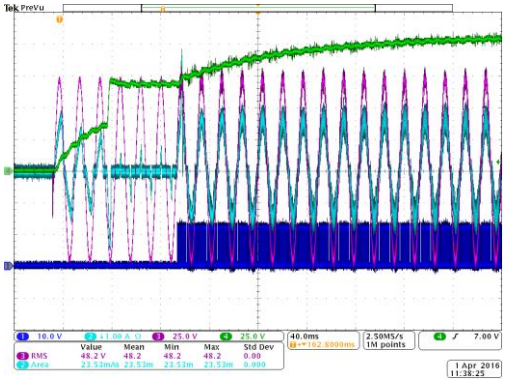
Uniquely qualified for use in CCM Totem Pole PFC due to excellent Body Diode











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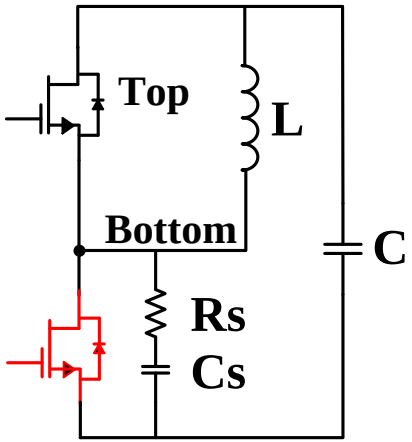
Snubber Design for UF3C120080K4S series



Test Conditions

- Top switch is the freewheeling device
- VDS, ID are measured for the bottom switch
- VGS: +15V turn on, -5V turn off
- Rgon 10Ω, Rgoff 10Ω
- VDS 800V
- ID: 25A
- Temperature: 120°C both top & bottom switch
- Snubber: 10Ω, 220pF
- When adding a snubber, switching loss includes both device and snubber loss.
- DUT: UF3C120080K4S

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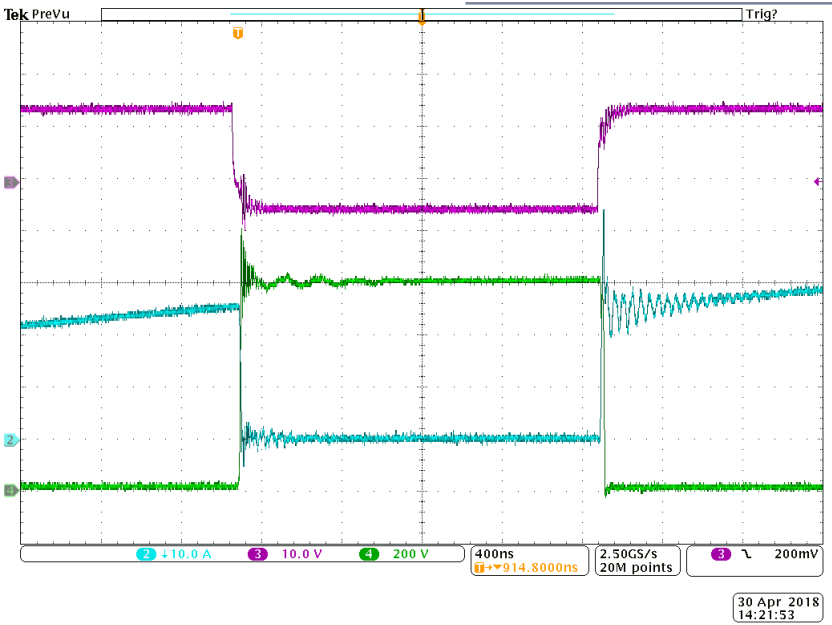
Snubber Design for UF3C120080K4S series

No Snubber, 25A, 800V, 120°C



Time: 400ns/div ID: 20A/div VGS: 10V/div VDS: 200V/div

- The measurement on the left shows more VDS ringing at turn-off transient than turn-on.
- Therefore the snubber should be placed on the bottom switch.

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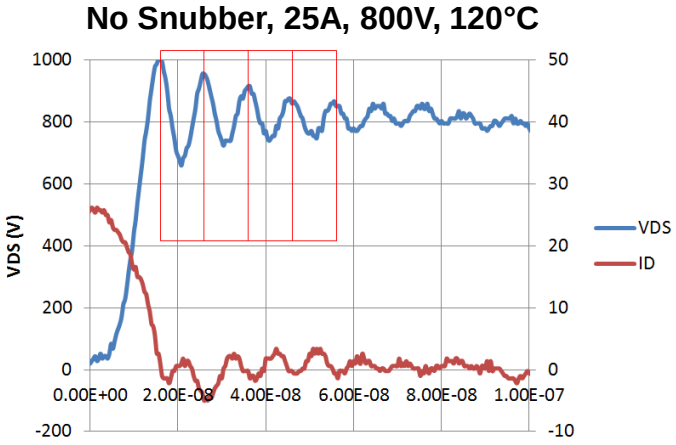
Snubber Design for UF3C120080K4S series

Guideline for snubber design



Time: 20ns/div ID: 10A/div VDS: 200V/div

The Cadd is a ceramic capacitor rated at 220pF. At 800V the ceramic capacitor capacitance is around 150pF which is also close to Cs = 148pF. Hence, Cs is the same as Cadd.

The VDS ringing frequency is **100MHz** (f0).

Adding a Cadd (220pF) reduces frequency to 42MHz (f1).

Therefore the circuit stray capacitance CLK is 47.1pF.

$$CLK = \frac{Cadd}{(f0/f1)^2 - 1}$$

Therefore the circuit leakage inductance LLK is 54nH.

$$LLK = \frac{1}{(2\pi f0)^2 CLK}$$

If damping factor ζ = 1.6, **Rs = 10Ω**

$$Rs = \frac{1}{2\zeta}\sqrt{\frac{LLK}{CLK}}$$

If cutoff frequency fc = 68.5MHz, **Cs = 220pF**.

$$Cs = \frac{1}{2\pi Rs fc}$$

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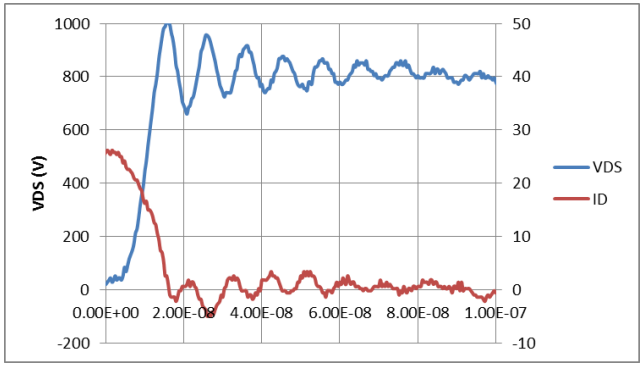
Snubber Design for UF3C120080K4S series

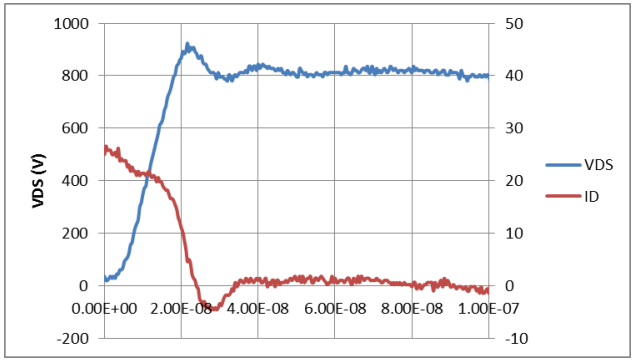
Trade off's using a snubber

No Snubber
Eon = 363uJ, Eoff = 64uJ



Time: 20ns/div ID: 10A/div VDS: 200V/div

With Snubber
Eon* = 371uJ, Eoff* = 147uJ



The Eon*, Eoff* with snubber are the total loss of device and snubber.

- Cascode turn-off ringing may be reduced by high Rgoff but this leads to long delay times
- Quick and easy solution to use fast SiC devices in existing designs without causing excessive ringing

UnitedSiC

Customer Reference: Micropower

- Phase shifted Full bridge
  - Need for an excellent body diode
- 10kW battery charger
- Technological partnership
- RESULTS:
  - 30% higher output power with UnitedSiC FET in same dimensions
  - Easy to replace Si-FET replacement using standard gate drive
  - 1.5% higher efficiency

MICROPOWER GROUP™
POWERFUL SOLUTIONS PARTNER

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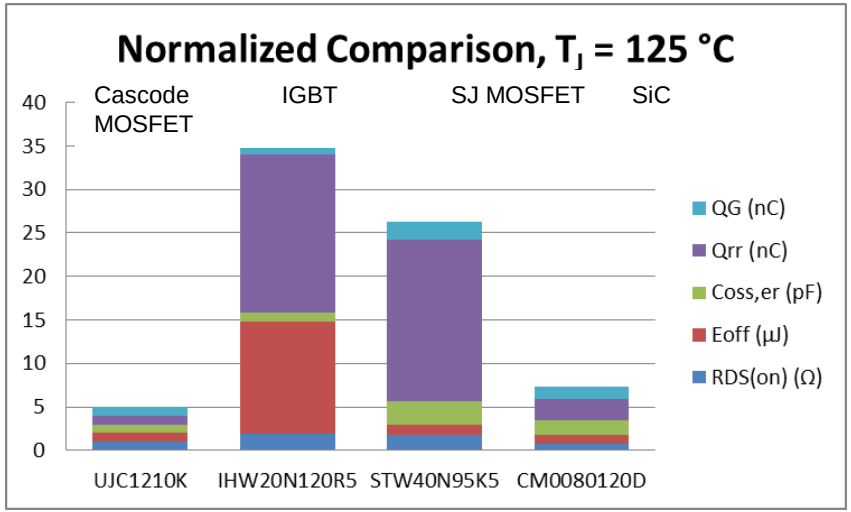
UnitedSiC FET advantage in PSFB



- Previous technologies include IGBT, super-junction MOSFET, and SiC MOSFET
- IGBTs have very high turn-off switching power loss, slow-switching reverse diode
- Super-junction MOSFETs have larger chip size, slow-switching reverse diode
- SiC MOSFET has larger chip size, asymmetric gate drive (-5 to 18 V typically)
- UnitedSiC FET is the best performing PSFB switch

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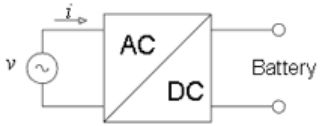
Battery Charger topology

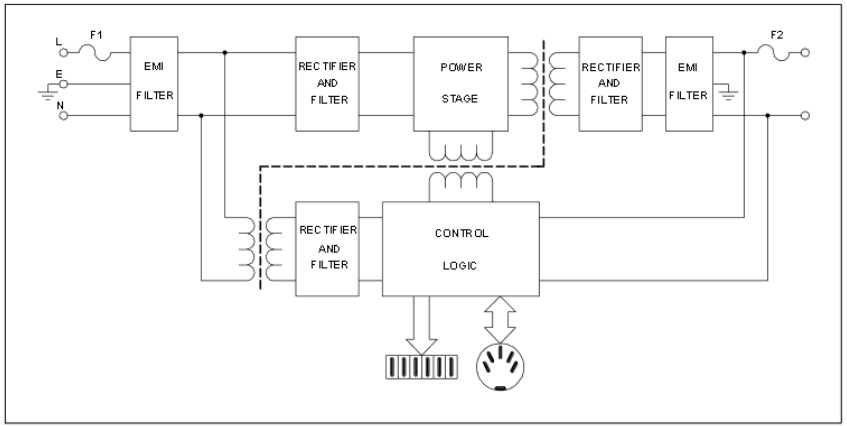
A non controlled traditional battery charger (rectifier) provides a simple direct **AC/DC conversion**



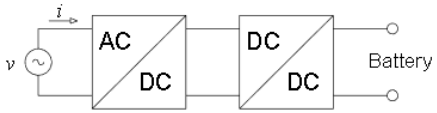
Disadvantages of this solution are:

- Low efficiency
- Large physical size
- Long charge times
- Charge depends on changes in the mains supply (with overcharge danger in the final charge phase)

Block Scheme



In modern battery chargers these disadvantages are solved with an **indirect AC/DC** conversion, by passing through an intermediate DC/DC conversion.



This is the usual method of operation for the SMPS (Switching Mode Power Supply) at high power. This solution gives a good performance for minimum costs and physical dimensions using switches more faster and powerful (modern technology).

The main advantages of this solution are:

- High efficiency
- Reduced dimensions
- Short charge times
- Charge independent from the changes of the mains supply
- Electronic control that provides the desired charge curve

Source: http://www.energicplus.com/content/manuals/Manual-NG1-single-phase-high-frequency-charger.pdf

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