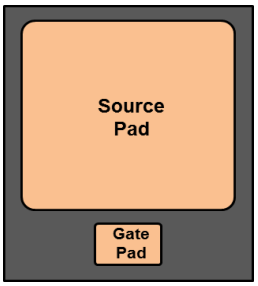
Description

United Silicon Carbide, Inc offers the high-performance G3 SiC normally-on JFET transistors. This series exhibits ultra-low on resistance ($R_{DS(ON)}$) and gate charge (Q_G) allowing for low conduction and switching loss. The device normally-on characteristics with low $R_{DS(ON)}$ at V_{GS} = 0 V is also ideal for current protection circuits without the need for active control, as well as for cascode operation.



Part Number	Package
UJ3N120070	Undiced wafer
UJ3N120070Z	Die on tape

Features

- Typical on-resistance $R_{DS(on),typ}$ of 70mΩ
- Voltage controlled
- Maximum operating temperature of 175°C
- Extremely fast switching not dependent on temperature
- Low gate charge
- Low intrinsic capacitance
- RoHS compliant

Typical Applications

- Over current protection circuits
- DC-AC inverters
- Switch mode power supplies
- Power factor correction modules
- Motor drives
- Induction heating

Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	V_{DS}		1200	V
Gate-source voltage	V_{GS}	DC	-20 to +3	V
		AC (1)	-20 to +20	
Continuous drain current (2,3)	I_D	T_C = 25°C	33.5	A
		T_C = 100°C	24.5	A
Pulsed drain current (3,4)	I_{DM}	T_C = 25°C	85	A
Maximum junction temperature (5)	$T_{J,max}$		175	°C
Operating and storage temperature	T_J, T_{STG}		-55 to 175	°C

(1) +20V AC rating applies for turn-on pulses <200ns applied with external $R_G > 1\Omega$.
(2) Limited by $T_{J,max}$
(3) Assumes a maximum junction-to-case thermal resistance of 0.59°C/W
(4) Pulse width t_p limited by $T_{J,max}$
(5) Package limited

Electrical Characteristics (T_J = +25°C unless otherwise specified)

Typical Performance - Static

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Drain-source breakdown voltage	BV_{DS}	V_{GS}= - 20V, I_D=1mA	1200			V
Total drain leakage current	I_D	V_{DS} = 1200V, V_{GS} = -20V, T_J = 25°C		5	30	µA
		V_{DS} = 1200V, V_{GS} = -20V, T_J = 175°C		18		
Total gate leakage current	I_G	V_{GS}=-20V, T_j=25°C		5	50	µA
		V_{GS}=-20V, T_j=175°C		20		
Drain-source on-resistance	$R_{DS(on)}$	V_{GS}=2V, I_D=10A, T_J = 25°C		63		mΩ
		V_{GS}=0V, I_D=10A, T_J = 25°C		70	90	
		V_{GS}=2V, I_D=10A, T_J = 175°C		139		
		V_{GS}=0V, I_D=10A, T_J = 175°C		154		
Gate threshold voltage	$V_{G(th)}$	V_{DS} = 5V, I_D = 35mA	-14	-11.5	-6	V
Gate resistance	R_G	f = 1MHz, open drain		3.3		Ω

Typical Performance - Dynamic (Refer to the datasheet of the packaged device UJ3N120070K3S)

Parameter	symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Input capacitance	C_{iss}	V_{DS} = 100V, V_{GS} = -20V, f = 100kHz		985		pF
Output capacitance	C_{oss}			100		
Reverse transfer capacitance	C_{rss}			95		
Effective output capacitance, energy related	$C_{oss(er)}$	V_{DS} = 0V to 800V, V_{GS} = -20V		52		pF
Total gate charge	Q_G	V_{DS}=800V, I_D = 25A, V_{GS}=-18V to 0V		116		nC
Gate-drain charge	Q_{GD}			63		
Gate-source charge	Q_{GS}			11		
Turn-on delay time	$t_{d(on)}$	V_{DS}=800V, I_D=25A, Gate Driver =-18V to 0V, $R_{G,EXT}$ = 1Ω, Inductive Load, FWD: UJ2D1215T T_J = 25°C		17		ns
Rise time	t_r			25		
Turn-off delay time	$t_{d(off)}$			29		
Fall time	t_f			39		
Turn-on energy	E_{ON}			434		µJ
Turn-off energy	E_{OFF}			393		
Total switching energy	E_{TOTAL}			827		
Turn-on delay time	$t_{d(on)}$	V_{DS}=800V, I_D=25A, Gate Driver =-18V to 0V, $R_{G,EXT}$ = 1Ω, Inductive Load, FWD: UJ2D1215T T_J = 150°C		17		ns
Rise time	t_r			23		
Turn-off delay time	$t_{d(off)}$			25		
Fall time	t_f			24		
Turn-on energy	E_{ON}			418		µJ
Turn-off energy	E_{OFF}			278		
Total switching energy	E_{TOTAL}			696		

Typical Performance Diagrams

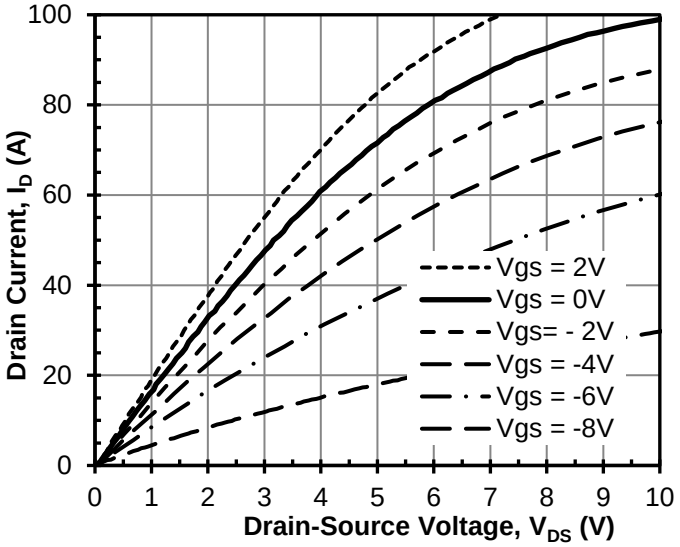


Figure 1 Typical output characteristics at T_J = -55°C

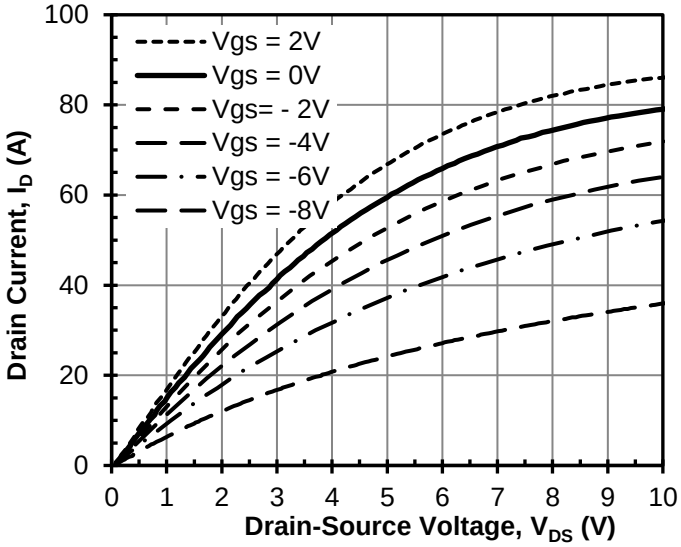


Figure 2 Typical output characteristics at T_J = 25°C

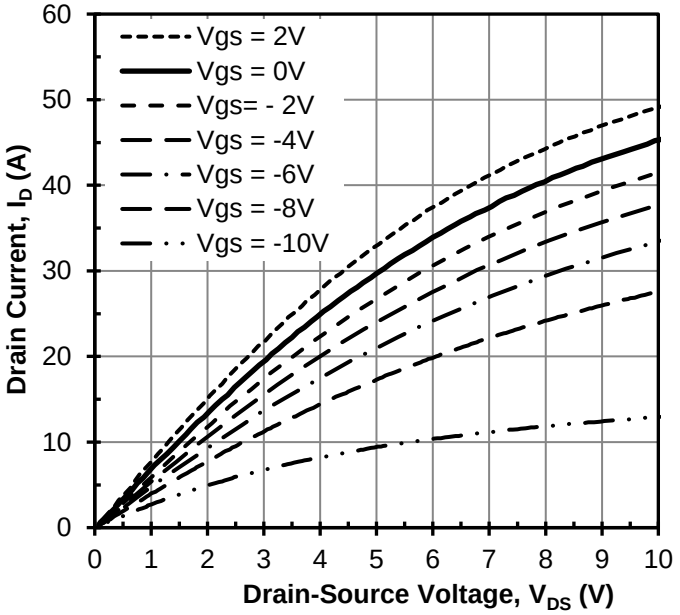


Figure 3 Typical output characteristics at T_J = 175°C

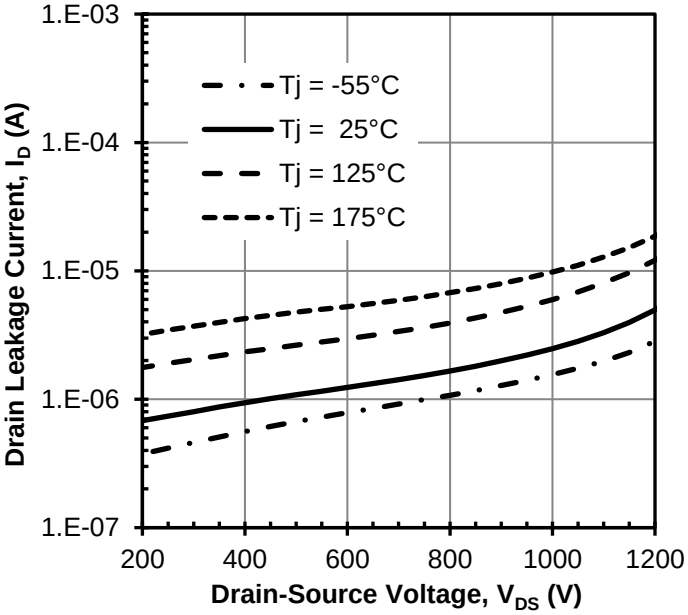


Figure 4 Typical drain-source leakage at V_{GS} = -20V

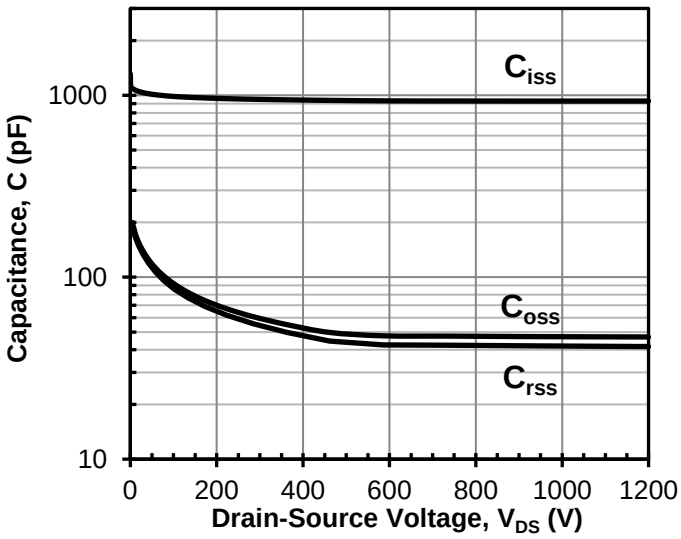


Figure 5 Typical capacitances at 100kHz and V_{GS} = -20V

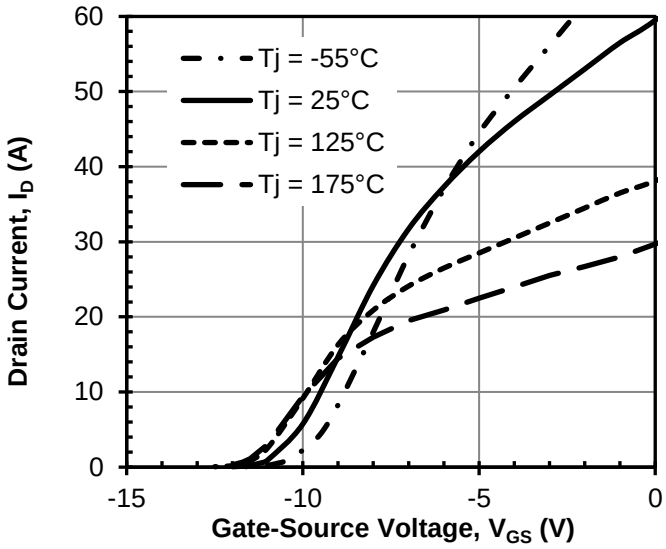


Figure 6 Typical transfer characteristics at V_{DS} = 5V

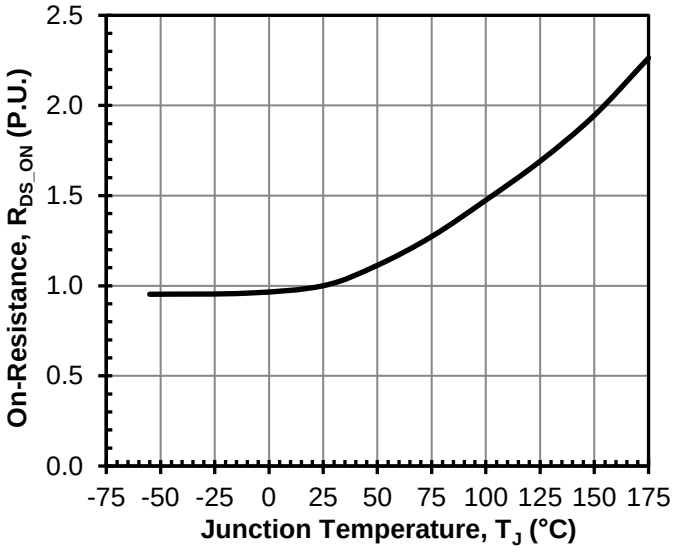


Figure 7 Normalized on-resistance vs. temperature at V_{GS} = 0V and I_D = 10A

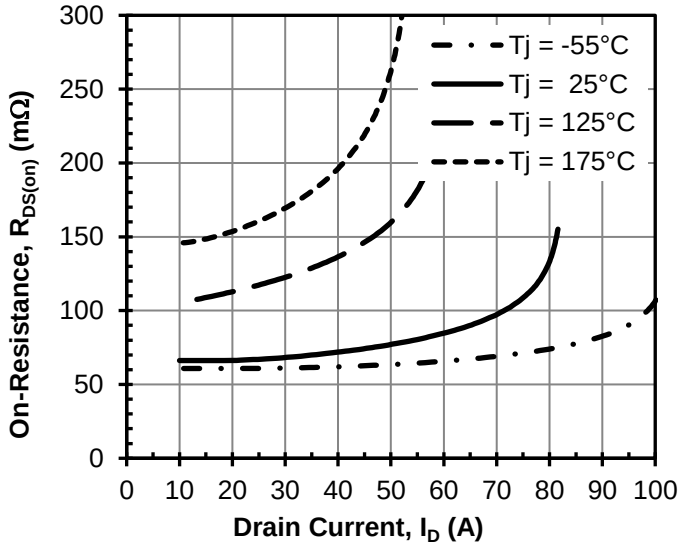


Figure 8 Typical drain-source on-resistance at V_{GS} = 0V

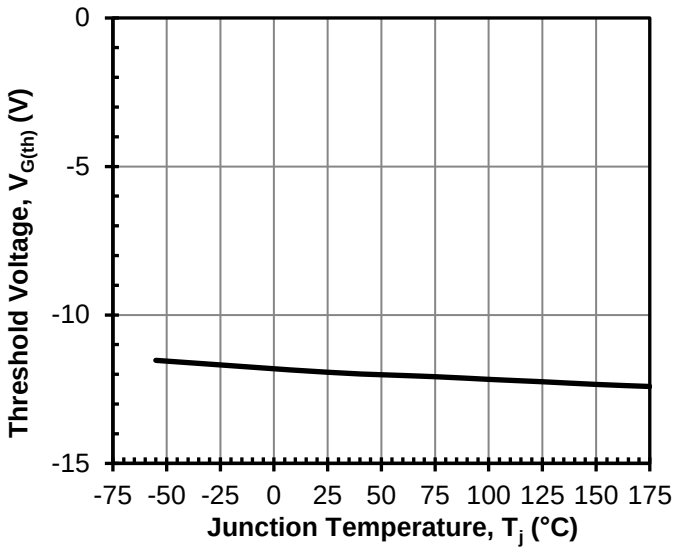


Figure 9 Threshold voltage vs. Tj at V_{DS} = 5V and I_D = 35mA

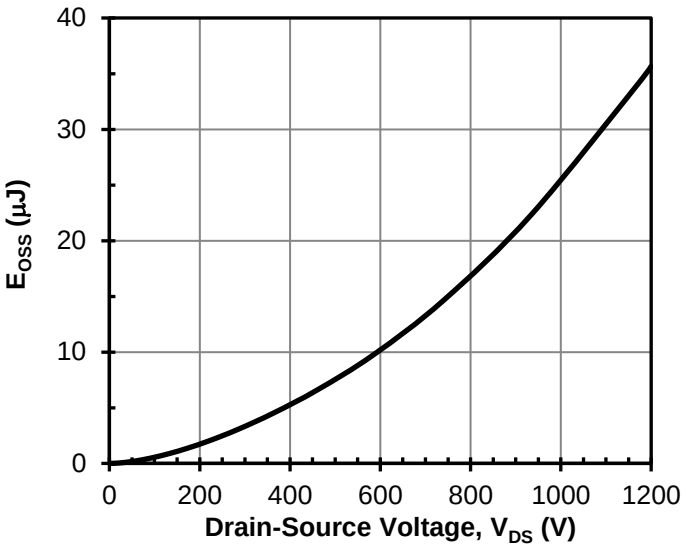


Figure 10 Typical stored energy in C_{OSS} at V_{GS} = -20V

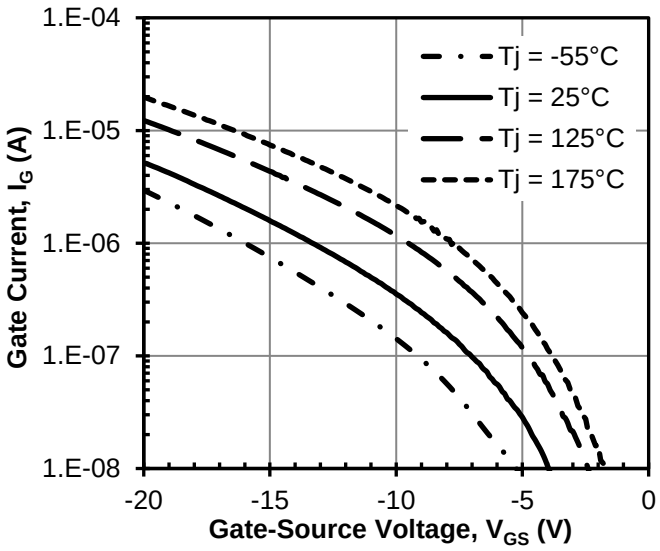


Figure 11 Typical gate leakage current at V_{DS} = 0V

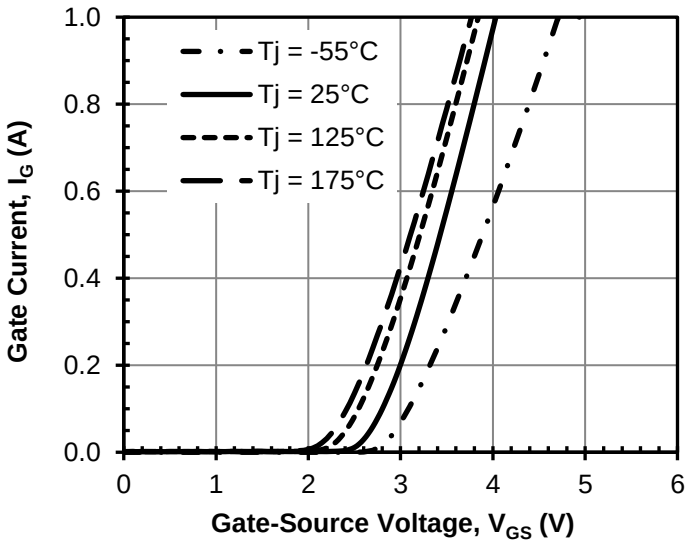


Figure 12 Typical gate forward current at V_{DS} = 0V

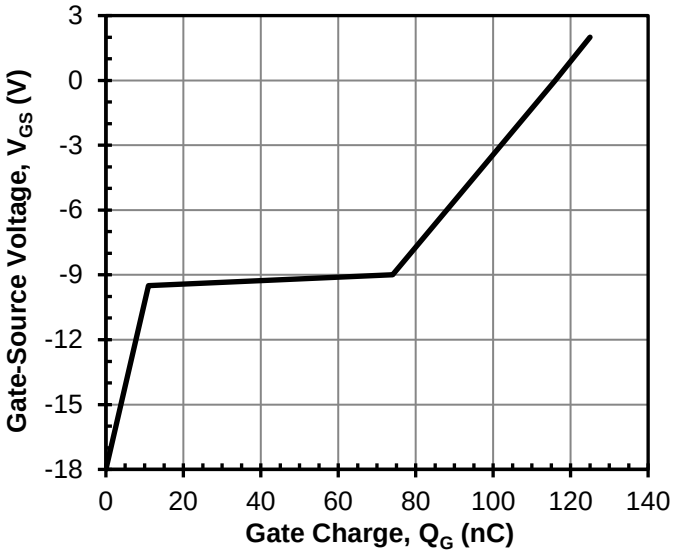


Figure 13 Typical gate charge at V_{DS} = 800V and I_D = 25A

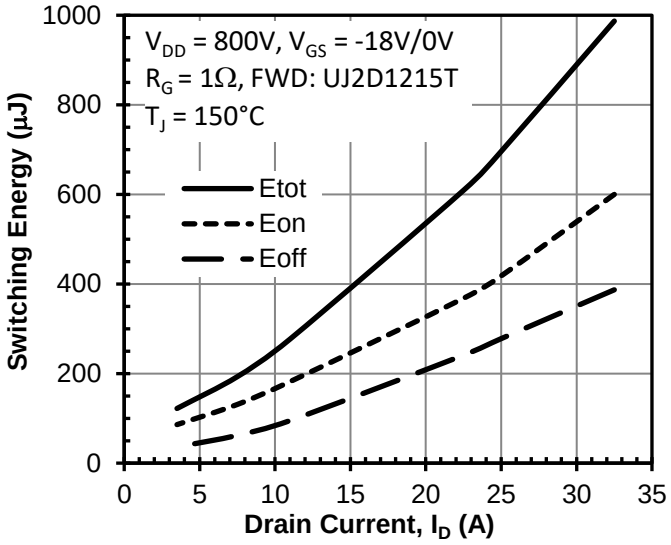


Figure 14 Clamped inductive switching energy vs. drain current at T_J = 150°C

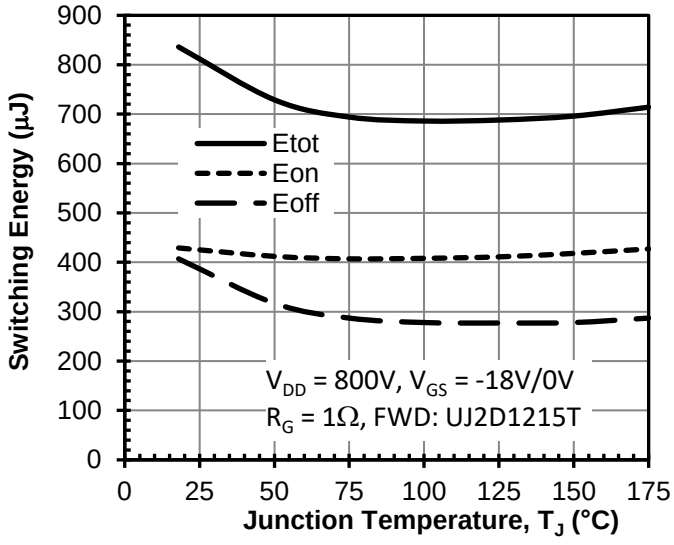


Figure 15 Clamped inductive switching energy vs. junction temperature at I_D = 25A

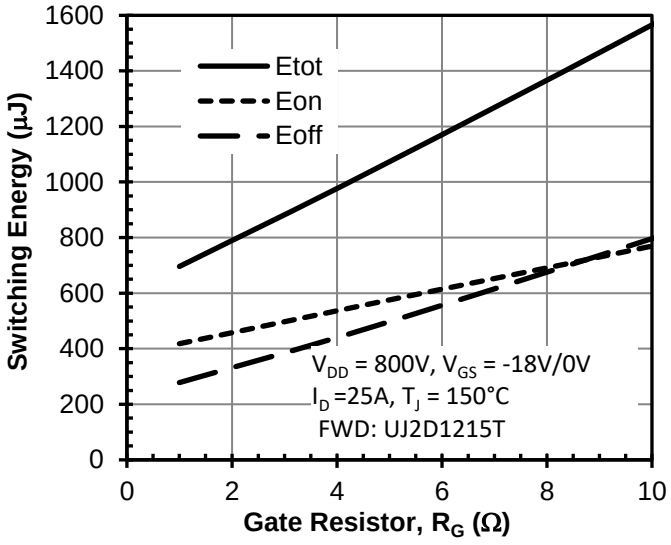
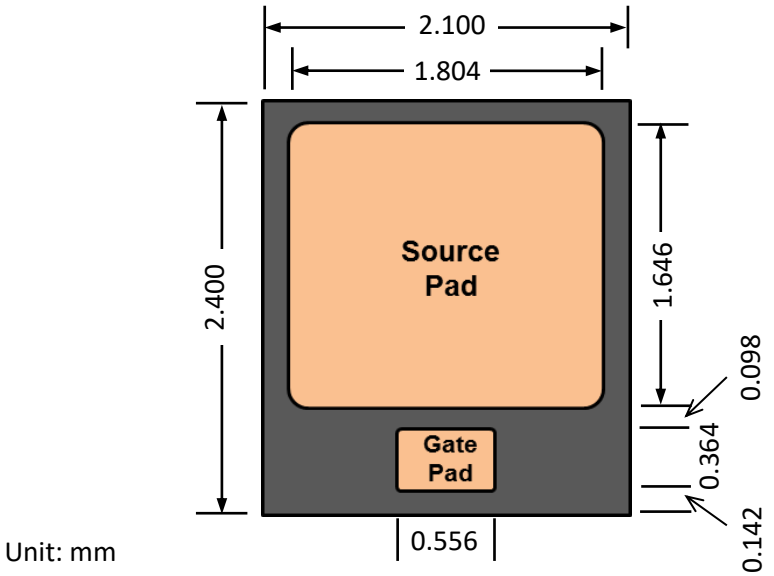


Figure 16 Clamped inductive switching energy vs. gate resistor R_G

Mechanical Characteristics

Parameter	Typical Value	Units
Die Dimensions with Scribe Line (L x W)	2.100 x 2.400	mm
Scribe Line width	80	µm
Source Pad Metal Dimensions (L x W)	1.804 x 1.646	mm
Gate Pad Metal Dimensions (L x W)	0.556 x 0.364	mm
Source Metallization (AlCu)	5	µm
Gate Metallization (AlCu)	5	µm
Backside Drain Metallization (Ti/Ni/Ag)	0.1/0.2/1	µm
Frontside Passivation	Polyimide	
Die Thickness	150	µm
Wafer Size	150	mm
Gross Die Per Wafer	2,795	

Chip Dimensions



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